CHAPTER 9

CONCLUSION

9.1 General

The UPQC system is successfully designed and modeled using the circuit elements of simulink. The sag in the voltage is created by applying an additional heavy load at the receiving end. This sag is compensated by using the DVR part of UPQC. The simulation results are in line with the predictions. The THD in the output is reduced by operating the inverter at 250 Hz. The hardware is fabricated and tested using PIC micro controller. The experimental results closely agree with the simulation results.

The eight bus system with UPQC is successfully designed and modeled using the circuit elements of simulink. The sag in the voltage is created by applying an additional heavy load at the receiving end. This sag is compensated by using DVR. The simulation results are in line with the predictions. The THD in the output is reduced by UPQC.

The fourteen bus system is drawn by using the corresponding data. This is simulated and the results are presented. The results indicate that the power quality is improved by introducing UPQC. The thirty bus system is simulated and the corresponding results are given. Multiple UPQCs are proposed to maintain the required voltage.

The fifty bus system is also simulated and the corresponding results are given. Multiple UPQCs are proposed to maintain the required voltage.
9.2 Scope for further work.

The scope of this work is the modeling and simulation of eight bus, fourteen bus, thirty bus and fifty bus systems. Simulation of sixty four bus system is yet to be done.

The simulation is done using Matlab. The simulation can be repeated with PSCAD or PSIM for comparison purpose. The hardware is done using PIC. The hardware may be implemented using DSP processor.