CHAPTER 5

CONCLUSIONS AND FUTURE SCOPE

5.1 Conclusions

WiMAX is an emerging wireless communication system that can provide broadband access with large coverage area. In the present work an effort is made to reduce the cost of WiMAX system. From the study of literature related to WiMAX systems, it is concluded that DUC and DDC are integral part of a WiMAX system. Study also shows that interpolator and decimator filters required for DUC and DDC consumes significant hardware resources. So an efficient design in term of filter structure/configuration/architecture of DUC and DDC can lead to an efficient and low cost WiMAX system.

According to WiMAX standards, WiMAX systems can be designed for different channel bandwidth like 3.5 MHz, 5 MHz and 10 MHz. As higher bandwidth can lead to more data rate and also design of digital systems at large bandwith is of great challenge. So, in this thesis interpolator and decimator stages of WiMAX DUC and DDC are designed for 10 MHz bandwidth. According to WiMAX standards, for 10 MHz channel bandwidth, DUC and DDC need to be designed for interpolation and decimation factor of 8, and during their design, the spectral emission standards should be strictly followed.

Comparison among FIR and IIR filters show that due to their less implementation complexity, linear phase and stability, FIR filters are better choice than IIR filters. From the comparative study of various FIR filter design techniques like window based FIR filter design, frequency sampling based FIR filter design, maximally flat FIR filters design, equiripple FIR filter design, minimum mean square error FIR filter design, minimum phase FIR filter design and Nyquist FIR filter design, it is concluded that due to their low
implementation complexity, equiripple FIR filter design and Nyquist FIR filter designs can be used in the design of efficient interpolation and decimation filters.

From discussions among various filter structures like direct form structures and polyphase form structures, it has been concluded that the computational efficiency of any filter structure is determined by the number of multiplications per output sample. As compared to the conventional FIR interpolator structure, the direct form structure as well as polyphase structure reduces the number of multiplications by interpolation or decimation factor. Polyphase structures can exhibit the coefficient symmetry. Thereby polyphase configuration can be suitable for the savings in memory. Also as compared to the polyphase filter structures, the direct form filter structures have the advantage that they can easily be modified by using symmetry property of FIR filters. So, to take the advantages of both implementations, the proposed interpolators and decimators have been implemented with direct form polyphase structure.

In the proposed work, interpolation and decimation filters are designed using both equiripple FIR filter design and Nyquist FIR filter design methods using direct form polyphase structure. These designs are implemented using single stage, two stages and three stages. From comparison of the resources utilized for each kind of implementation, it is concluded that both for interpolation and decimation filters, Nyquist FIR filter design requires less number of resources. Although it was observed that resources utilized by two stage design are slightly more as compared to three stage design, but due to less FPGAs implementation complexity a two stage interpolator and two stage decimator with Nyquist design is used for the proposed low cost WiMAX DUC and DDC.

FPGAs provide an ideal implementation platform for developing broadband wireless systems. To accelerate the performance of these broadband systems, state of the
art high end and high performance FPGAs are available. Using logic blocks and programmable routing resources, FPGAs can be configured to implement custom hardware functionality. As FPGAs are completely reconfigurable, so they can be reprogrammed for new applications. The availability of high level design tools by different vendors has resulted in small design cycle on an FPGA. Also FPGAs are truly parallel in nature, different processing operations do not have to compete for the same resources. Each independent processing task is assigned to a dedicated section of the chip and can function autonomously without any influence from other logic blocks. DA can be explored to save resources in FPGA implementation of DSP functions. DA can be used to trade memory for combinatory elements, resulting in low cost LUT based FPGAs implementation. Also the designer can select a serial or parallel DA implementation to trade off speed and resource utilization.

In the proposed design of interpolation and decimation filters for DUC and DDC, DA architecture is used. Different configurations for serial and parallel implementations are presented and compared to trade off between speed and resource utilization. Stratix II GX FPGA device are used for implementing the interpolation and decimation filters. To utilize the resources of the targeted Stratix II GX, its internal architecture is discussed in detail. Mathematical analysis of serial and parallel implementation of DA FIR filter is also presented to show area and speed tradeoff between these two kinds of implementations. From the discussions, it is concluded that parallel implementation calculates the filter output in a single clock cycle as compared to serial implementation, which require clock cycles equal to the input data width to calculate an output. This additional speed for parallel implementation comes at the expense of large FPGA area.

The DUC and DDC for WiMAX system is designed using Nyquist FIR filter design with direct form polyphase structure. The Proposed DUC is implemented by
cascading pulse shaping single rate FIR filter, interpolation by 2 filter and interpolation by 4 filter, and DDC are implemented by cascading, decimation by 4 filter and decimation by 2 filter and decimation channel filters. All these filters are implemented with both fully serial and fully parallel architectures with different serial units and pipeline levels respectively.

From comparison among the various types of architectures, implemented for pulse shaping, interpolation by 2 and interpolation by 4, decimation by 4, decimation by 2 and decimation channel filters, it is concluded that fully parallel DA architecture with pipeline level of 1 has high speed with moderate area requirement. So, for design of interpolation filters for WiMAX DUC and decimation filters for WiMAX DDC, fully parallel DA architecture with pipeline level of 1 will result in low cost WiMAX system with improved performance.

5.2 Scope for Future Work

For designing a multistage filter, the development of a reliable method to find the number of optimum number of stages may be future area of concern. In addition to design of individual stages of interpolator or decimator, future work may be on the design of low cost and efficient direct digital synthesizer and mixer also. The work done in this thesis may be extended for other broadband communication systems.