CHAPTER 1

INTRODUCTION

1.1 Introduction and Motivation

Modern signal processing problems are often solved in the digital domain due to the availability of powerful very large scale integrated (VLSI) circuits which allow to perform complex operations in real time, without the well known shortcomings of analog implementations. The source signal filtering, shaping, mixing etc., is done in the digital domain and only the final result is converted back to analog. A very important and fundamental operation in discrete time signal processing is sampling. Discrete time signals are often obtained from continuous time signal by simple sampling. This is mathematically modeled as the evaluation of a function of a real variable at discrete values of time. Physically, it is a more complicated and varied process which might be modeled as convolution of the sampled signal by a narrow pulse. In several applications, it is sometimes necessary to convert a signal from one sample rate to another sample rate. An input can be down sampled or up sampled before processing to ease the computational load, or sometimes two units must be connected whose respective sample rates do not match.

To overcome the degradation caused by analog to digital (A/D) and digital to analog (D/A) conversion, all processing blocks must have digital interfaces. Depending on the available bandwidth of the channel, the required quality, and the data rate of the interfaces a wide variety of sample rates are used. The incorporation of all these systems is however trouble-free, if a suitable sample rate converter is used at each interface in the field of communications systems (Crochiere, R. E. and Rabiner, L. R., 1975). (Meyer,
Multirate signal processing is a key tool used in these signal processing applications. Digital filters are a key part of multirate signal processing. Digital filters are required to bandlimit the spectrum of the signal to the prescribed bandwidth in accordance with the actual sampling rate. In sampling rate conversion systems, filters are used in decimation to suppress aliasing and in interpolation to remove imaging. Since an ideal frequency response cannot be achieved, so the performance of the system for sampling rate conversion is mainly determined by the filter characteristics. Thus an appropriate filter design is required for sampling rate conversion with minimum signal distortion.

Many types of sampling have been discussed in the literature (Linden, D. A., 1959), (Feldbauer, M., et al., 2006), (Crochiere, R.E. and Rabiner, L.R., 1981) including non-uniform sampling, uniform sampling, and multiple function uniform sampling. For uniform sampling, the sampling period \( T \) and the sampling rate \( F \) can be shown as:

\[
F = \frac{1}{T}
\]  

It is necessary that the sampling rate \( F \) be chosen to satisfy the requirements of the Nyquist sampling theorem. The sampling rate \( F \) is a fundamental consideration in many signal processing techniques and applications. It often determines the convenience, efficiency, and accuracy in which the signal processing can be performed. The process of digitally converting the sampling rate of a signal from a given rate \( F = \frac{1}{T} \) to a different rate \( F' = \frac{1}{T'} \) is called sampling rate conversion. When the new sampling rate is higher than the original sampling rate, the process is called interpolation, whereas when the new sampling rate is lower than the original sampling
rate, the process is called decimation. Figure 1.1 provides a general description of a sampling rate conversion system.

\[
x(n) \rightarrow g_m(n) \rightarrow y(m)
\]

**Figure 1.1: Basic process of digital sampling rate conversion**

The ratio of sampling periods of \( y(m) \) and \( x(n) \) can be expressed as a rational fraction,

\[
\frac{T'}{T} = \frac{F}{F'} = \frac{M}{L}
\]

where \( M \) represents decimation factor and \( L \) represents interpolation factor.

For linear time varying systems, each output sample \( y(m) \) can be expressed as a linear combination of input samples \( x(n) \). Mathematically \( y(m) \) can be expressed as (Rabiner L.R., et al., 1975):

\[
y(m) = \sum_{n=-\infty}^{\infty} g_m(n) x([Mm/L] - n)
\]

**Figure 1.2: Basic representation of Up Sampling**
In the trivial case when $T' = T$, or $L = M = 1$, equation (1.4) reduces to the simple time-invariant digital convolution equation

$$y(m) = \sum_{n=-\infty}^{\infty} g(n)x(m-n)$$  \hspace{1cm} (1.5)

1.2 Literature Review

Wireless broadband data communication is experiencing a rapid expansion. To keep up with this noteworthy growth in the demand for wireless broadband, new technologies and architectures are needed to greatly improve system performance and network scalability while significantly reducing the cost of equipment. With increasing cost pressures on wireless equipment makers, there is a significant drive to reduce both capital expenditure and operating expenditure cost attributes of the communication systems. Worldwide Interoperability for Microwave Access (WiMAX), is an emerging wireless communication system that can provide broadband access with large coverage area (Kejie, L. et al., 2007).

The basic building blocks in WiMAX systems are entities that either increase or
decrease the sampling rate called interpolator and decimator respectively. As discussed earlier in section 1.1, the change in sampling rate of a signal has direct impact on its spectrum, therefore sample rate changes are preceded or followed by a frequency selective filter.

In this thesis, the main aim is to design and implement a low cost WiMAX system. To attain this goal, the design of cost efficient and optimal performance filters for interpolation and decimation may be of main concern. So detailed literature is reviewed to explore the design techniques, which can lead to the development of efficient and low cost interpolation and decimation filters.

Almost all filter banks perform the operations of upsampling, linear filtering and downsampling, and therefore belong to a class of linear, periodically time varying systems (Vetterli, 1987). Due to its linear, time varying property, it is possible to change the ordering of these operations (Vaidyanathan, 1990). Multirate filter design, under various aliasing and cross-talk free constraints has been a main focus of study in filter bank theory, and it is mostly modeled through matrix notations (Vetterli, 1987). Compared to individual single channel filters, the filter banks are efficient signal processing structures both in terms of design and computation (Vaidyanathan, 1993). Still the implementation cost may be a significant factor in the implementations of modern communication systems. (Dick, Chris and Harris, Fred, 1998) Chris dick & Harris have developed important system options made available to the designer as spin-offs of the derivation. They have derived the Farrow filter which supports continuously variable resampling. A fractional delay filter is a device for performing band limited interpolation between the samples of a time series. The Farrow filter is a multirate filter structure that offers the
option of continuously adjustable delay. But this will be useful only for the applications having fractional sample rate conversion.

(Goslin, G.R., 1995) Goslin has elaborated the importance of FPGAs for application specific applications. FPGAs have become a competitive alternative for high performance DSP applications, previously dominated by general purpose DSP and ASIC devices (Crochiere and Rabiner, 1976).

Knowing the fact that a multistage design is efficient than its single stage counterpart, both computationally and with respect to memory's requirements, the objective is to determine the optimal number of stages for a particular sample rate change factor. The determination of number of stages in a multirate filter design has been formulated and solved as an optimization problem (Crochiere and Rabiner, 1975). Optimal multistage design with respect to computations also leads to a design with the least memory storage requirements (Crochiere and Rabiner, 1976). This is due to the fact that storage requirements mostly depend on the filter order which strongly effects the number computations per seconds, therefore minimizing computations also optimizes the design with respect to storage requirements. Although this approach results in less memory requirement, yet it does not provide a method by which the filter can be implemented with fewer resources on an FPGA.

(Dick Chris & Haris Fred, 1999) Chris has investigated an architectural option for constructing an interpolation filter with integer factor using Xilinx FPGA technology. Although the proposed architecture helps in saving the device logic resources as compared to other techniques that provide the same functionality, yet this architecture is limited to narrow band filters only. Lokken proposed sample rate conversion (SRC) with separate source and sink clock signals (Lokken, I., 1999). Although such SRC can provide very good jitter rejection, but still it encorporate some distortion and noise to the signal.
Cascaded Integrated Comb (CIC) filters are a class of digital FIR filters typically used for integer SRC (Hogenauer, 1981). The simplest CIC filter is composed of a comb stage and an integrator stage. The CIC architecture can be used for both interpolation and decimation. In the CIC filter design, passband response and stopband rejection characteristics are governed by three integer parameters, number of stages, the differential delay and number of bits in input/output registers. For instance, higher the number of stages, higher will be the available stopband attenuation. CIC filters are multiplication free filters with limited storage requirements which make them ideal for high speed data converters. Significant efforts have been made to build multirate solutions based on CIC filters (Hentschel and Fettweis, 2000b). It is more conducive to use multistage CIC filters for large decimation ratios (Saud, A.A. and Stuber, 2003). To offer better alias rejection, a modified CIC filter design has been proposed in (Saud, A.A. and Stuber, 2003). But this improvement in performance comes at the cost of more computational and memory overhead.

Conventional CIC filters exhibit high passband droop. A separate FIR filter is required to compensate this droop. Jiang proposed a filter sharpening technique to improve passband characteristic of CIC filters by using multiple copies of the same filter (Jiang and Jr., 1997). Once again, this filter sharpening comes at the cost of excessive computations per second for the higher order CIC filters. A similar approach to CIC filter sharpening has been proposed with an efficient structure (Dolecek and Mitra, 2005). For a factorizable integer decimation factor, a two stage realization has been proposed with filter sharpening using multiple copies performed in the second stage at low sampling rate, while the first stage of comb filters is polyphase decomposed to gain efficiency. It was assumed that the CIC filter response can be decomposed into separate comb and integrator sections for a specific decimation ratio. But this assumption may not hold in practice for multi-standard digital communication systems.

Oh et al has proposed a low complexity approach for CIC compensation. In this
approach, low order frequency domain polynomials are used to improve the passband response (Oh et al., 1999). A drawback of this scheme is the increase in computational cost for higher order polynomials (more than four).

Vaidyanathan has proposed filter design technique based on $M^{th}$ band filters (Vaidyanathan, 1993). Because of its simple design techniques, half-band filters ($M$th band filters with $M=2$) is a popular choice. The coefficients of a half-band filter can easily be obtained using traditional algorithms (Mitra, 2000). The half-band filters appear in conjunction with CIC and linear phase FIR filters to complete sample rate converter design (Jiang and Jr., 1997), (Yeung and Chan, 2004) and (Oh et al., 1999). But the half band filter implementations are more useful in the multistage applications, when the rate change can be factored by 2.

A class of multi-rate filters namely polynomial interpolation filters has also been used for an efficient implementation with digital techniques to correct symbol timings and effect of band-limited communication channel in the communication receivers (Erup et al., 1993). Band limited channels results in inter symbol interference (ISI). This ISI can be mitigated by transmitting the symbols, which are pulse shaped by a root raised cosine filter that limits the frequency contents of source symbols. Before pulse shaping, the transmitted symbols are oversampled. A number of multirate realizations help to combine pulse shaping and interpolation at a fraction of the cost compared to the complexity of traditional interpolation operations (Harris, 2005). Yoon, S.H. presented a hybrid structure of a transposed direct form (TDF) and direct form filter (DF) based on the flattened coefficients method so that it can reduce the number of flip-flops and full-adders without additional critical path delay (Yoon, S.H. et al., 2004). A resource sharing method and sharing-pattern searching algorithm has been also presented to reduce the number of adders without deepening the logic depth. Still the proposed structure is not efficient from
FPGA implementation point of view.

The polyphase filter bank based, digital upconverter and digital downconverter has been presented in (Kiessling and Mujtaba, 2002). In this work, a generalized polyphase filter bank incorporating sample rate alterations has been used as a wideband digital upconverter at the transmitter and a corresponding filter bank does the inverse operations at the receiver. But the flexibility of proposed architecture is limited to a particular standard since the sampling frequency is dependent on channel spacing and standard's baseband symbol rate. While it eliminates the need of separate sample rate converters after channelization, but this method increases the rate of computations in the filter bank in order to achieve arbitrary sample rate conversion (Harris et al., 2003).

The strict operational conditions imposed by polyphase discrete fourier transform (DFT) filter bank and its limitations, that it is usable with only one standard at a time led Saud and Stuber (Saud, A.A. and Stuber, 2004) to employ complex modulated perfect reconstruction (PR) filter banks. In their proposed scheme, the wideband input signal containing variable bandwidth channels has been decomposed into sub-channels. The sub-channels have been grouped into mutually exclusive sets with a particular channel extracted by reconstructing the corresponding subbands set through the synthesis filter bank by a suitable coding scheme. The disadvantage of this scheme is the information required by different synthesis sections to determine the subband components that combine to form a user channel. To an extent, it also hampers the flexibility of the design since it caters variable bandwidths but the user channel location within the subband are still fixed. Moreover, when compared to the uniform DFT filter bank where aliasing cancellation amplitude and phase distortion problems are absent, the Signal to Noise Ratio (SNR) performance of PR channelizer may be higher with the same number of taps in the prototype filter. Although a polyphase form of the PR filter bank channelizer has also been
derived, but it is applicable only for the number of channels greater than 15. Floyd, M. has described an implementations, which is particularly convenient in a practical hardware (Floyd M. Gardner et al., 1993). Simulations demonstrate that simple interpolator gives excellent performance. In many cases, two-point, linear interpolation is adequate. If better performance is needed, classical four points, third-order polynomials could be used. Better yet, a novel four-point interpolating filter with piecewise-parabolic impulse response can have performance superior to that of the standard cubic interpolator and still be implemented much more simply.

Quite a few techniques have been covered in literature on direct conversion (Abidi, 2007). Direct conversion does not involve the digital IF stage. The aliasing is sometimes referred to as under-sampling, which has been explained in (Seo et al., 2003). It was shown that if the IF frequency and sampling frequency of a band-limited user channel is selected suitably, it is possible to downconvert this channel without complex multiplications, provided the sampling frequency is at least twice the user channel bandwidth. Since switching among different clocks can introduce jitters in the signal (Arkesteijn et al., 2006) so a single clock is desirable in any digital communication system. Moreover, a single clock system has lower power consumption as compared to a digital communication system with multiple clocks (Hentschel and Fettweis, 2000b). Dengwei Fu has developed a novel interpolation method which instead of approximating the continuous-time signal with a conventional polynomial and computing the synchronized samples using a Farrow structure, uses a trigonometric polynomial (Dengwei Fu & Alan N. Willson, 1999). Simulation results indicate that improved performance reduced computational delay and in most cases, simplified hardware can be achieved. The method was formulated in terms of a digital interpolation filter. It has been
shown that with a slight modification of original method, the interpolation filter based on the trigonometric polynomial can achieve a desired frequency response.

A multi-standard sample rate conversion (SRC) solution was proposed in (Hentschel, T. and Fettweis, G. 2000) where a Farrow structure performed fractional SRC after initial decimation using FIR filters. Decimation before Farrow structure reduced the sampling rate so that polynomial filters computations are performed at the low sampling rate end. However, it is not always possible to shift polynomial interpolation to the lowest sampling rate since arbitrary decimation prior to it can result in aliasing errors.

A DDC architecture (Savvopoulos, P. and Antonakopoulos, T., 2007) have been designed and implemented, which can be integrated into the next generation software radio receivers. The presented DDC module is based on two cascaded stages of frequency conversion, operating on samples fed by an A/D converter of moderate sampling frequency. The DDC contains also a SRC unit which performs decimation on the resulting inphase and quadrature (I/Q) samples for proper interfacing with demodulator logic at lower rates. An efficient way to implement flexible multirate signal processing systems with high oversampling ratio and adjustable fractional or irrational sampling rate conversion ratio has been considered in (Babic, D. et al., 2001). The proposed decimation filter consists of parallel cascaded integrator comb (CIC) filters followed by a linear interpolation filter. The idea is to use two parallel CIC filters to calculate the two needed sample values for linear interpolation. These samples occur just before and after the final output sample, but this corresponds to a system where the linear interpolation is done at the higher input sampling rate. Due to this high rate, implementation complexity may increase. In addition, although it can be used in a multi-standard communication receiver which should be adjustable for different symbol rates, yet sometimes there may be
problem of symbol rate synchronization. Chapman has shown that the implementation of
digital filters with sample rates above just a few MHz are generally difficult and expensive
to realize using standard digital signal processing (Chapman, K., 1996).

DA can play very important part in an effective FPGA implementation (Chang,
T.S. and Jen.C.W., 1999). It is an efficient mechanism to trade combinational logic with
memory for high performance computation. DA can significantly help to save area in DSP
hardware design. DA replaces the explicit multiplications by ROM look-ups, which is an
efficient technique to implement on FPGAs.

From literature review, it can be seen that interpolator and decimator for sample
rate conversion, play crucial role at physical layer operation in digital communication
system and consumes significant hardware resources, so an efficient design in term of
filter structure/configuration/architecture of these blocks can contribute to make an
efficient and low cost communication system. Then by using the FPGA architecture in the
efficient way, performance can be improved. In addition to this, further improvements can
be achieved with the help of DA using suitable structural implementation.

1.3 Problem Formulation

WiMAX is an emerging technology with significant potential that is poised to
revolutionize the broadband wireless internet access market. As wireless broadband data
communication is experiencing a rapid expansion. To keep up with this noteworthy growth
in the demand for wireless broadband, new technologies and architectures are needed to
greatly improve system performance and network scalability while significantly reducing
the cost of equipment. With increasing cost pressures on many wireless equipment
makers, there is a significant drive to reduce both capital expenditure and operating
expenditure cost of the communication systems infrastructure. The significant
requirements for these systems include low cost in terms of lesser silicon area, power
consumption, processing speed, flexibility etc. Digital Up Converters (DUC) and Digital Down Converters (DDC) are very important and integral part of a WiMAX system. As they utilize the major resources, therefore better design and implementation of DUC and DDC can result in low cost WiMAX system with improved performance.

1.4 Objectives

The literature analyzed provided that there is scope for the design and implementation of Digital Up Converter & Digital Down Converter, which should lead to a low cost WiMAX system with improved performance. To accomplish this task the following objectives are formulated:

- To study the WiMAX system, standards and its applications.
- To study the literature related to the efficient design and implementation of various Signal Processing modules required in a WiMAX system.
- To explore the design space between the WiMAX algorithms and their architecture leading to the development of a low cost WiMAX system with improved performance.

1.5 Research Methodology

DUC and DDC modules are implemented in Matlab and Simulink environment. After verifications of their functionality, these modules are coded using hardware description languages (HDLs) for calculating the resources utilized by the proposed modules on FPGA. Because of their capability to integrate the various design phases by combining the algorithm development, simulation, synthesis and verification capabilities, the system level design tools like DSP system builder is used.

1.6 Organization of the Thesis
The thesis is organized in five chapters. Chapter 1 presents the introduction and motivation, literature review, problem formulation, objectives of the thesis and organization of the thesis.

Chapter 2 describes the WiMAX communication system. In this chapter first an overview of WiMAX system is given. Then WiMAX standards are elaborated and specifications for DUC and DDC are derived. This chapter also explains the importance of DUC and DDC to be used in WiMAX system.

Chapter 3 analyzes the filters, their structures, and interpolation & decimation designs. In this chapter methods are analyzed to get the efficient design of interpolation and decimation filters. For this filter classes are explored for interpolation and decimation filters. The interpolation and decimation filters, with single stage and multistage techniques are also designed. By comparing the different filter configurations, implementation cost for interpolation and decimation filters are evaluated. Based on the analysis of filter designs, efficient filter configurations are proposed for WiMAX DUC and DDC.

In chapter 4, FPGA implementation and DA are explored to get the efficient system with improved performance. In this chapter basic FPGA architecture is discussed in detail. The concepts of DA for our design are explored for different serial and parallel implementations. Different techniques for reducing ROM are elaborated. Then efficient FIR filter is designed using the DA, in which concept of sum of product (SOP) is used to make the design multiplier free. At the end interpolation and decimation filters for WiMAX DUC and DDC are implemented with different serial and parallel architectures.

In chapter 5 results have been discussed in detail. The scope for future work is also discussed in this chapter.