CHAPTER 1
INTRODUCTION

1.1 MOTIVATION AND PROBLEM STATEMENT:

Increasing the performance is the best criterion for developing any communication system. The work presented here is aimed at increasing the speed & performance of the OFDMA (Orthogonal Frequency-Division Multiple Access) modulator and demodulator. The developed OFDMA communication structure is then targeted to the OFDMA based WiMAX (Worldwide Interoperability for Microwave Access) communication modules, for increasing their efficiency by utilizing Field Programmable Gate Array (FPGA) based Fast Fourier Transform (FFT) algorithm.

The work focuses at proposing a new Radix-2^2 Algorithm and its utilization in OFDM (Orthogonal frequency-division multiplexing) based communication systems. Hardware oriented pipelined architecture called Radix-2^2 Single Path Delay Feedback (R2^2SDF) algorithm is developed by integrating a twiddle factor decomposition technique in divide-and-conquer approach to form a spatially regular Signal Flow Graph (SFG). Mapping the algorithm to the cascading delay feedback structure leads to the proposed architecture [1]. This algorithm has the same multiplicative complexity as the radix-4 algorithm, but retains the butterfly structure of radix-2 algorithm.

This algorithm need to be coded VERILOG Hardware Description Language (Verilog) and targeted into an FPGA for its implementation. After implementation, the FPGA module is to be introduced into the OFDM modulator and demodulator comparing the efficiency of the Radix-2^2 algorithm with that of the Radix-4 algorithm. This OFDM module should then be implemented into the Fixed and Mobile WiMAX communication modules, proving that the efficiency of the communication modules increases with the new OFDMA implementation.
1.2 OBJECTIVE:

The objective of our thesis is proposing a new Radix-2\(^2\) Algorithm and its utilization in OFDM based communication system. The modified OFDM communication system has been implemented and the Fixed WiMAX and Mobile WiMAX systems are redesigned for better results. The design has been done in AGILENT’S ADVANCED DESIGN SYSTEM (ADS) software.

Our proposed work is implemented with VERILOG. The code is synthesized and targeted into Xilinx Spartan3 FPGA. This FFT module is used in OFDM communication system to improve its performance. The improved OFDM modules are then implemented in fixed and mobile WiMAX communication systems which utilize OFDMA technique for their communication. The advantages, performance, and timing of the communication modules after implementation of the proposed technique are then discussed towards the end, giving a scope for the manufacturing of efficient WiMAX communication modules. A comparison is also made for the implementation of the fixed and mobile WiMAX, with the proposed architecture and that of the Radix -4 architecture. The comparison clearly indicates that the WiMAX with the proposed architecture is efficient than the other implementations of its kind.

In recent years, OFDM technique has paying attention in the standardization of performance in communication system. When compared to single-carrier schemes, OFDM has the ability to cope with severe channel conditions without complex equalization filters. Now-a-days OFDM has developed into a widespread structure for wideband digital communication. In many communication systems such as Asymmetric Digital Subscriber Line (ADSL), Wireless Local Area Network (WLAN) or multimedia communication services are utilized the OFDM technology.

OFDM is a proficient technique for high-speed digital transmission over multipath fading channels. OFDM has been recently regarded to be a promising technique for the future mobile communications. OFDM technology is used for many communication systems and multimedia communication services. OFDM has been adopted for various transmission systems such as Wireless Fidelity (WIFI),
WIMAX, Digital Video Broadcasting (DVB), Long Term Evolution (LTE) and more.

OFDM technique is a multicarrier modulation technique with a rather simple implementation performed using FFT/IFFT (Inverse Fast Fourier Transform) algorithms, and robust against frequency-selective fading channels which is obtained by converting the channel into flat fading sub-channels [1]. The FFT is one of the key components in OFDM system. There are more and more communication systems requiring higher points FFT and higher symbol rates. The requirement establishes challenges for low power and high speed FFT design with large points. FFT also finds applications in linear filtering, digital spectral analysis and correlation analysis, etc.

1.3 BACKGROUND STUDY:

Within the last two decades, communication advances have reshaped the way we live our daily lives. In this new information age, high data rate and strong reliability in wireless communication systems are becoming the dominant factors for a successful exploitation of commercial networks [2]. The most recent eras in the communication side is wireless communications, which remake our day-to-day lives. Wireless communications is a rapidly growing area in the present booming communications industry, which having the potential of providing high-speed and high-quality information exchange between portable devices. Now-a-days computer plays a dynamic part in our daily lifetime. Internet also places a major part in changing the lifestyle of people such as work, communication, play and learns.

The basic idea of OFDM is to divide the available spectrum into several orthogonal sub channels so that each narrowband sub channels experiences almost flat fading allowing sub channels in the frequency domain thus increasing the transmission rate [3]. OFDM is a flexible and bandwidth-efficient modulation technique which has the capability to combat ISI, because OFDM systems divide a wide-band channel profile into many narrowband orthogonal sub channels, each carrying a Quadrature Amplitude Modulation (QAM) symbol [4]. In dispersive
environment broadband access, OFDM is considered to be an efficient modulation technique.

OFDMA is a multiple access scheme that enables the coexistence of multiple users whose data streams are modulated according to the OFDM technique. OFDMA subdivides the available system bandwidth into multiple orthogonal frequency subcarriers in the frequency domain and into symbol periods in the time domain. In each symbol period, the serial input data stream of a specific user is divided into parallel data streams and each stream modulates a specific subcarrier.

Each user occupies a subset of the available frequency subcarriers in the band, which enables the coexistence of multiple users in the same frequency band. In this way, user-specific data substreams are created that are orthogonal in frequency and time. Each of the parallel streams is associated with a lower data rate than the original user’s serial input data stream [4]. OFDM technology is used in any communication systems and multimedia communication services.

The main advantages of OFDM are its spectrum efficiency and robustness against fading in multipath propagation. Reflection signals in OFDMA change the phase and amplitude of information symbols and this influence is compensated by pilot signals [5].
One of the key components in OFDM system is the FFT. There are more and more communication systems requiring higher points FFT and higher symbol rates. The requirement establishes challenges for low power and high speed FFT design with large points. With this developed OFDMA based WiMAX, which is used in telecommunications protocol that provides fixed and mobile Internet access. The present WiMAX revision provides up to 40 Mbit/s, whereas IEEE 802.16m update expected to offer up to 1 Gbit/s fixed speeds.

WiMAX—which stands for Worldwide Interoperability for Microwave Access—is bringing the wireless and Internet revolutions to portable across the globe. WiMAX is providing the capabilities of the Internet, without any wires, to every living room, portable computer, phone, and handheld device. The WiMAX modules utilize the OFDMA scheme in their physical layer of communication.

The OFDM modulation is cost effectively realized by the Inverse Fast Fourier Transform (IFFT) that enables the use of a large number of subcarriers—up to 1024 according to the Mobile WiMAX system profiles—to be accommodated within each OFDMA symbol. Prior to transmission, each OFDMA symbol is extended by its cyclic prefix followed by digital-to-analog (D/A) conversion at the
transmitter. At the receiver end, after analog-to-digital (A/D) conversion, the cyclic prefix is discarded and OFDM demodulation is applied through the FFT.

The FFT algorithm eliminates the redundant calculation which is needed in computing Discrete Fourier transform (DFT) and is thus very suitable for efficient hardware implementation [6]. A high level implementation of a high performance FFT for OFDM modulator and demodulator is presented in this work. The design has been coded in Verilog and targeted into Xilinx Spartan3 field programmable gate arrays. Radix-2$^2$ algorithm [7] is proposed and used for the OFDM communication system. The design of the FFT is implemented and applied to fixed WiMAX–IEEE 802.16d and mobile WiMAX–IEEE802.16e communication standards. The results are tabulated and the hardware parameters are compared. The improved OFDM module is implemented in fixed and mobile WiMAX communication systems which utilize OFDMA technique for their communication, with advantages in terms of performance, and timing of the communication modules.

A handful of researches are available in increasing the speed and performance of OFDM by proposing new algorithm for FFT and some of them are discussed and reviewed in the upcoming session of this section.

1.4 FFT PROCESSOR

Pipeline FFT processor is a specified class of processors for DFT computation utilizing fast algorithms. It is characterized with real-time, non-stopping processing as the data sequence passing the processor.

In this thesis, a new approach for real-time pipeline FFT processor, the Radix-2$^2$ Single-path Delay Feedback, or R2$^2$SDF architecture will be presented. We will begin with a brief review of previous approaches. A hardware oriented radix-2$^2$ algorithm is then developed by integrating a twiddle factor decomposition technique in divide and conquer approach to form a spatially regular signal flow graph (SFG). Mapping the algorithm to the cascading delay feedback structure leads to the proposed architecture.
1.5 REVIEW OF FFT IMPLEMENTATIONS

The architecture design for pipeline FFT processor had been the subject of intensive research as early as in 70’s when real-time processing was demanded in such application as radar signal processing, well before the VLSI technology had advanced to the level of system integration. Several architectures have been proposed over the last 2 decades since then, along with the increasing interest and the leap forward of the technology. Here different approaches will be put into functional blocks with unified terminology, where the additive butterfly has been separated from multiplier to show the hardware requirement distinctively. The control and twiddle factor reading mechanism have been also omitted for clarity. All data and arithmetic operations are complex, and a constraint that N is a power of 4 applies.

**R2MDC:** Radix-2 Multi-path Delay Commutator [8] was probably the most straightforward approach for pipeline implementation of radix-2 FFT algorithm. The input sequence has been broken into two parallel data stream flowing forward, with correct “distance” between data elements entering the butterfly scheduled by proper delays. Both butterflies and multipliers are in 50% utilization. \( \log_2 N \)-2 multipliers, \( \log_2 N \) radix-2 butterflies and \( 3/2N-2 \) registers (delay elements) are required.

**R2SDF:** Radix-2 Single-path Delay Feedback [9] uses the registers more efficiently by storing the butterfly output in feedback shift registers. A single data stream goes through the multiplier at every stage. It has same number of butterfly units and multipliers as in R2MDC approach, but with much reduced memory requirement: \( N-1 \) registers. Its memory requirement is minimal.

**R4SDF:** Radix-4 Single-path Delay Feedback [10] was proposed as a radix-4 version of R2SDF. The utilization of multipliers has been increased to 75% due to the storage of 3 out of radix-4 butterfly outputs. However, the utilization of the radix-4 butterfly, which is fairly complicated and contains at least 8 complex adders, is
dropped to only 25%. It requires $\log_4 N - 1$ multipliers, $\log_4 N$ full radix-4 butterflies and storage of size $N-1$.

**R4MDC:** Radix-4 Multi-path Delay Commutator [8] is a radix-4 version of R2MDC. It has been used as the architecture for the initial VLSI implementation of pipeline FFT processor and massive wafer scale integration. However, it suffers from low, 25%, utilization of all components, which can be compensated only in some special applications where four FFTs are being processed simultaneously. It requires $3\log_4 N$ multipliers, $\log_4 N$ full radix-4 butterflies and $5/2N-4$ registers.

**R4SDC:** Radix-4 Single-path Delay Commutator [11] uses a modified radix-4 algorithm with programmable 1/4 radix-4 butterflies to achieve higher, 75% utilization of multipliers. A combined Delay-Commutator also reduces the memory requirement to $2N-2$ from $5/2N-1$, that of R4MDC. The butterfly and delay-commutator become relatively complicated due to programmability requirement. R4SDC has been used recently in building the largest ever single chip pipeline FFT processor for high definition television application.

A swift skimming through of the architectures listed above reveals the distinctive merits of the different approaches: First, the delay-feedback approaches are always more efficient than corresponding delay-commutator approaches in terms of memory utilization since the stored butterfly output can be directly used by the multipliers. Second, radix-4 algorithm based single-path architectures have higher multiplier utilization, however, radix-2 algorithm based architectures have simpler butterflies which are better utilized. The new approach developed in following sections is highly motivated by these observations.

**Proposed:** The most desirable hardware oriented algorithm will be that it has the same number of non-trivial multiplications at the same positions in the SFG as of radix-4 algorithms, but has the same butterfly structure as that of radix-2 algorithms. Another algorithm combining radix-4 and radix-‘4 + 2’ in DIT form has been used to
decrease the scaling error in R2MDC architecture, without altering the multiplier requirement. The clear derivation of the algorithm in DIF form with perception of reducing the hardware requirement in the context pipeline FFT processor is, however, yet to be developed.

In this work, a hardware-oriented radix-$2^2$ algorithm is derived which has the radix-4 multiplicative complexity but retains radix-2 butterfly structure in the SFG. Based on this algorithm, a new, efficient pipeline FFT architecture, the R2$^2$SDF architecture, is put forward. The validity and efficiency of the proposed architecture has been verified by extensive simulation.

**1.6 IMPLEMENTATION OF PROPOSED FFT IN OFDM AND DESIGN USING AGILENT’S ADS:**

The fundamental principle of the OFDM system is to decompose the high rate data stream (bandwidth=$W$) into $N$ lower rate data streams and then to transmit them simultaneously over a large number of subcarriers [7]. The IFFT and the FFT are used for modulating and demodulating the data constellations on the orthogonal subcarriers respectively [12].

The proposed OFDM based Fixed WiMAX communication system is designed in Agilent’s Advanced Design System. The FIXED WiMAX 802.16d and MOBILE WiMAX 802.16e were implemented in ADS for different values of N. The power measurements and the timing measurements are tabulated in the previous chapter for N=256. A random signal was applied to the design of FIXED WiMAX as well as MOBILE WiMAX design. Initially the design is implemented and synthesized with Radix-4 FFT, after that the design is modified with proposed FFT.

The accurate power and timing measurements have been made for various values of N. The results have been tabulated and compared for the same design using Radix-4 FFT and for proposed FFT. The observations clearly indicate that the communication system with proposed FFT is almost two times faster for higher values of N. Also, there is a considerable change in the overall power consumption of the system. Since the system design in AGILENT’s ADS is presented, the outcome of this thesis can be directly used for manufacturing the prototype.
The outcome of this work has several potential applications in the field of communication systems. This efficient OFDM communication module, after its physical implementation, can be effectively utilized in the manufacturing of the Fixed and Mobile WiMAX communication systems as discussed in this work. Further, the implementation can also be extended to any other communication standards that use OFDM technique in the architecture. Apart from implementation into the OFDM communication module, the proposed Radix $2^2$ algorithm can be implemented in other communication modules that utilize FFT, and increase their efficiency to a great extent.