CHAPTER 3

POWER QUALITY ENHANCEMENT USING D-STATCOM AND APLC

3.1 INTRODUCTION

The use of power electronic systems with rectifier loads continue to increase leading to distorted current drawn from the mains resulting in low power factor and high THD. This distortion problem becomes more serious when the loads become highly nonlinear. Voltage variations are the most serious PQ disturbances for manufacturing industry caused by short circuit faults and energization of large loads. As a result, declining PQ in distribution systems has become an important issue in the present day. Hence, this chapter explores on the mitigation techniques using D-STATCOM and shunt active power line conditioner for compensating PQ related disturbances such as voltage variations and harmonics respectively.

3.2 D-STATCOM FOR VOLTAGE SAG AND SWELL MITIGATION USING DIODE-CLAMPED MULTILEVEL INVERTER

The mitigation of voltage variations such as voltage sags and swells has become one of the major issues for improving the power quality in distribution networks. In automated industries, the effects of voltage sag and voltage swell leads to production downtime and equipment damage. Custom power conditioners alleviate the problems of power quality. These are either
series active or shunt active filters. They are used in distribution system to provide better voltage regulation, near zero power interruptions, low harmonic voltages and to improve the power factor.

The recent trends are growing towards the use of Voltage Source Inverter (VSI) based custom power devices (Hingorani 1995 and Sannio 2003). The conventional two-level inverter has practical limitations in achieving higher output voltage. The use of series connection of devices to increase its rating would not result in better performances (Lara et al 2002 and Acha et al 2006). Multi-step inverters (Sunil Kumar et al 1999) are able to meet these requirements, but they suffer from the limitations of occupying large area, slow dynamic response and very expensive (Rufer et al 1995 and Lai et al 1996).

The multilevel inverters attempt to overcome some of the limitations addressed above and are found to be the most suitable for medium voltage and high power applications such as Static Compensator (STATCOM), Active Power Filter (APF) (Ying et al 2002) and motor drives. The Multilevel Diode-Clamped Inverter (MLDCI) is simple and easy to control (Rodriguez, 2002 and Jochen et al 2002). This configuration is reported to be an effective solution for voltage sourced converters connected to high voltage distribution networks and widely employed in several FACTS devices.

This section discusses the proposed five-level diode-clamped D-STATCOM for voltage sag and voltage swell mitigation using SPWM technique. The simulation results obtained are presented and discussed.
3.2.1 Multilevel Diode-Clamped Inverter

The multilevel diode-clamped VSI is preferred over the two-level VSI for high power applications as it reduces the Total Harmonic Distortion (THD) in Point of Common Coupling (PCC) voltage and source current for a given DC link voltage and inverter switching frequency.

3.2.1.1 Basic configuration

The simplest diode-clamped inverter is known as the Neutral Point Clamped converter (NPC) (Rashid, 2001). Figure 3.1 shows one phase of an m-level diode-clamped inverter. Node ‘p’ indicates the positive bus, Node ‘n’ indicates the negative bus and ‘o’ is the mid point of the DC bus. All the capacitor shown in the Figure 3.1 is of equal voltage rating. In Figure 3.1, the switching states $S_{a1}$, $S_{a2}$, $S_{a(m-2)}$ and $S_{a(m-1)}$ take the value 1 if the corresponding switch is conducting and 0 otherwise. For a five-level inverter, the switch combinations given in (Ramanarayanan 2004 and Rashid 2001) are used to synthesize the output voltage $V_{ao}$ of phase a with respect to the neutral point o. The five-level inverter parameters are given in Table 3.1.

Table 3.1 Five-level inverter parameters

<table>
<thead>
<tr>
<th>Inverter Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of main switches per leg</td>
<td>20</td>
</tr>
<tr>
<td>Device ON resistance (Ω)</td>
<td>0.01</td>
</tr>
<tr>
<td>Device OFF resistance (Ω)</td>
<td>1.0E6</td>
</tr>
<tr>
<td>Forward voltage drop (kV)</td>
<td>0</td>
</tr>
<tr>
<td>Forward break over voltage (kV)</td>
<td>1.0E5</td>
</tr>
<tr>
<td>Reverse withstand voltage (kV)</td>
<td>1.0E5</td>
</tr>
<tr>
<td>Snubber resistance (Ω)</td>
<td>500</td>
</tr>
<tr>
<td>Snubber capacitance (μF)</td>
<td>25</td>
</tr>
</tbody>
</table>
Figure 3.1 One phase leg of an m-level diode-clamped inverter

An m-level diode-clamped inverter requires (m-1) pairs of power semiconductor devices and 2(m-2) clamping diodes per phase leg in addition to (m-1) main DC capacitors of equal value. The number of switches to be turned ON at a time is (m-1) to produce m-level output phase voltage in the case of MLDCI. The line-to-line output voltage of the inverter varies from \(+V_{dc}\) to \(-V_{dc}\) and has (2m-1) levels in the output, while the phase voltage varies from \(+V_{dc}/2\) to \(-V_{dc}/2\) with m-levels. Of the various strategies developed to improve the output voltage waveform of a VSI multiple carrier method of Sinusoidal Pulse Width Modulation (SPWM) strategy is employed here. In this method, (m-1) triangular carrier signals \(V_c\) are compared with a controlled sinusoidal modulating signal \(V_m\). All of the carriers have the same frequency and amplitude. The carrier signal used is In Phase Sinusoidal Pulse Width Modulation (IP-SPWM). Hence the multilevel inverter is capable of generating a ‘more sinusoidal’ waveform with lower device ratings and required switching frequency. Increasing the carrier wave frequency further minimizes the percentage THD. The five-level diode-clamped inverter is simulated using PSCAD/EMTDC.
3.2.2 MLDCI based D-STATCOM

This section presents the MLDCI based custom power controllers such as D-STATCOM. The basic block diagram of the distribution system with multilevel D-STATCOM is shown in Figure 3.2. Although theoretically, it is possible to realize an m-level diode-clamped inverter, there exists few difficulties from the hardware implementation point of view. As the number of levels increases, the number of devices to be turned ON/OFF also increases. The generations of gating signals at higher carrier frequency becomes a difficult task resulting in narrow pulse width for each turn ON and turn OFF of the device. Also the practical issues such as capacitor voltage unbalance, unequal and high voltage rating for clamping diodes have restricted the maximum number of levels to five in the proposed work.

Figure 3.2 System under study with multilevel D-STATCOM

The proposed D-STATCOM configuration is based on a five-level VSI to regulate voltage at the PCC and the control is based on SPWM. The five-level VSI converts the DC voltage across the capacitor in to three phase
AC output voltage. This voltage is phase coupled with AC system through the reactance of the coupling transformer. By varying the phase and magnitude of the output voltage of D-STATCOM effective control of active and reactive power exchange between the D-STATCOM and the AC system is achieved. Voltage regulation and reactive power compensation are also achieved by controlling the multilevel VSI connected in shunt with the AC system.

3.2.2.1 SPWM control

The aim of the control scheme is to maintain the constant voltage at the PCC. The multilevel VSI switching strategy is based on the SPWM technique, which offers simplicity and good response. The PCC voltage regulator (PI controller) generates the required delay angle ‘\(\delta\)’. In the SPWM controller, the sinusoidal signal is phase modulated by means of the angle ‘\(\delta\)’ and firing pulses for the multilevel VSI is generated.

The main parameters of the SPWM scheme are the amplitude modulation index \(m_a\) of the modulating signal and the frequency modulation index \(m_f\) (integral multiple of the fundamental frequency 50 Hz) of the carrier signal. The \(m_a\) can vary from 0 to 1 per unit (p.u.). The carrier frequency of 450 Hz with \(m_f = 9\) is used here. For the balanced network, the firing pulses for the phases B and C are shifted by 120° and 240° respectively. The control implementation is kept very simple by using only voltage signal as the feedback variable in the control scheme. The \(K_p = 0.399\) and \(K_i = 0.750\) are used for the PI controller settings.

3.2.3 Results and Discussion

The main functions of the proposed D-STATCOM are reactive power compensation and the mitigation of voltage sag and swell. The test
system comprises of 230 kV transmission system, represented by Thevenin’s equivalent, feeding the primary side of transformer. A varying load of $(0.482 + j1.769)$ $\Omega$ is connected to the 11kV, secondary side of the transformer. A five-level D-STATCOM is connected through a coupling transformer to the 11kV secondary winding to provide instantaneous voltage support at the load point. An 800 $\mu$F capacitor on the DC side provides the required DC voltage for D-STATCOM.

The performance evaluation of the proposed multilevel D-STATCOM is investigated by the following test case conditions. The simulation results of the RMS voltage at the PCC for without and with five level diode-clamped D-STATCOM are shown in Figures 3.3 and 3.4(a) respectively. A zoom in the parts in which sag and swell occurred is shown in Figure 3.4(b) and (c) for evidencing the dynamic response of the system. During the simulation period of 0.3 to 0.6 sec, a step increase in load of 165 % is applied. In this case the RMS voltage drops by 25% with respect to the reference voltage value of 1.0 p.u. At 0.6 sec, the heavy load is withdrawn. In this case, the RMS voltage at the PCC is very close to the reference voltage value of 1.0 p.u. In the simulation period of 0.9 to 1.2 sec the capacitor banks are connected to the high voltage side of the network. In this case, the RMS voltage increases by 23% with respect to the reference voltage value of 1.0 p.u. The phase voltage at PCC during the voltage sag and swell for without and with D-STATCOM connected is shown in Figure 3.5 in order to give a better idea of the D-STATCOM performance.
Figure 3.3 RMS Voltage at PCC without D-STATCOM

Figure 3.4 (a) RMS voltage at PCC with D-STATCOM (b) Zoomed version of the RMS voltage during voltage sag (c) Zoomed version of the RMS Voltage during voltage swell
The source current and the D-STATCOM output current are shown in Figures 3.6 and 3.7 respectively. Referring to Figures 3.6 and 3.7, it is observed that the source current magnitude remains practically constant irrespective of the changes in the load as the D-STATCOM compensates for the reactive power requirement.
The performance of the system response for short duration voltage sag (0.4 sec - 0.5 sec) and voltage swell (1.0 sec – 1.1 sec) is tested and the results of the RMS voltage and phase voltage at PCC during short duration voltage sag and swell without and with D-STATCOM are shown in Figures 3.8 and 3.9 respectively. It is to be noted that the performance of the D-STATCOM is found to be satisfactory during short duration voltage sag and swell conditions. Referring to (Figures 3.4 to 3.9) it is noted that the D-STATCOM injects/absorbs reactive current so as to maintain the PCC voltage constant during voltage sag/swell conditions.
Figure 3.8 RMS voltages at PCC for short duration sag and swell
(a) Without D-STATCOM (b) With D-STATCOM
Figure 3.9  Phase voltage at PCC for short duration sag and swell
(a) Without D-STATCOM   (b) With D-STATCOM

Figure 3.10 Harmonic spectrum of PCC voltage with D-STATCOM
Figure 3.11 Harmonic spectrum of source current with D-STATCOM

It is found that the performance of five-level D-STATCOM is satisfactory in providing effective and continuous voltage regulation of the RMS voltage at the load point (PCC). When voltage sag occurs, the D-STATCOM supplies reactive power to the system. During voltage swell, the D-STATCOM absorbs reactive power in order to maintain the PCC voltage to the reference value (Figure 3.4). In spite of sudden load variations, the regulated RMS voltage shows a reasonably smooth profile, with less transient overshoot.

The magnitude of these transients is kept within $\pm 5\%$ with respect to the reference voltage and they do not last for more than two cycles. The PI controller settings works satisfactorily for 20% of impedance variations during voltage sag and 25% of capacitance variations during voltage swell conditions. The FFT analysis of PCC voltage and source current with the D-STATCOM is shown in Figures 3.10 and 3.11 respectively. The % THD for PCC voltage and source current have been computed and found to be 2.11% and 7.83% respectively. This indicates that the harmonics originated due to the switching action of the D-STATCOM is within the acceptable IEEE 519 limits.
3.3 FUZZY LOGIC BASED D-STATCOM FOR VOLTAGE SAG AND SWELL MITIGATION

Voltage sag and swell is considered as the most serious problem of power quality. It is often caused by faults in power systems or by starting of large induction motors. It interrupts or leads to malfunction of any electric equipment, which is sensitive to voltage variations. Therefore, the loss resulted due to voltage sag and swell problem for a customer at the load end is huge. D-STATCOM is recently being used as the active solution for voltage sag and swell mitigation. The two-level D-STATCOM with a conventional P-I controller (Lara et al 2002) is referred in this section as Conventional D-STATCOM (CD-STATCOM). The basic principle and operation of CD-STATCOM is same as MLDCI based D-STATCOM explained in section 3.2.2. The CD-STATCOM is used to prevent voltage sag and swell problems and it is normally designed based on a linearized model derived around some specific operating state. The crucial phase of design of such a CD-STATCOM is to tune its parameters to provide optimal performance at the chosen operating state. In large and complex power systems, robustness of controllers is of primary concern in order to ensure satisfactory performance at different operating conditions. Since, the robustness of the CD-STATCOM is limited, it requires re-tuning of its already tuned parameters to maintain acceptable performance at different operating states to which the power system is subjected.

The conventional PI controller of the CD-STATCOM is replaced by a fuzzy logic controller to obtain Fuzzy logic based D-STATCOM (FD-STATCOM). Fuzzy logic control is a simple but effective alternative control scheme to conventional control. FD-STATCOM does not require parameter re-tuning because of its inherent robustness. In this section, an FD-STATCOM is proposed and its effectiveness in the mitigation of voltage
sag and swell is investigated by applying to the test system discussed in section 3.2.3. The simulation results obtained using FD-STATCOM are presented and compared with that obtained using CD-STATCOM reported earlier by (Lara et al 2002).

The basic block diagram of the distribution system with FD-STATCOM is shown in Figure 3.12. The configuration of fuzzy logic controller is shown in Figure 3.13. The main input variable to the FD-STATCOM at the \( k^{th} \) time step is the deviation of load voltage magnitude, \( \Delta V(k) \) and is obtained from block-diagram shown in Figure 3.12.

\[
\Delta V(k) = V_{\text{err}}(k) = V_{\text{ref}} - V_{\text{actual}}
\]  

(3.1)

Another input variable to the FD-STATCOM is \( \dot{\Delta V}(k) \), the derivative of the load voltage magnitude deviation, which is generated from voltages measured at two successive sampling instants by using,

\[
\dot{\Delta V}(k) = \frac{(\Delta V(k) - \Delta V(k-1))}{\Delta T}
\]  

(3.2)

where \( \Delta T = \) Sampling interval

The output variable at the \( k^{th} \) time step is the change in phase angle \( \Delta \delta(k) \) required for driving the load voltage error to zero. In the SPWM controller, the sinusoidal signal is phase modulated by means of the angle \( \delta(k) \) and generates the switching pulses for the multilevel VSI. The output of FD-STATCOM at \( k^{th} \) time step is given by:

\[
\delta(k) = \delta(k-1) + \Delta \delta(k)
\]  

(3.3)
Figure 3.12 System under study with FD-STATCOM

Figure 3.13 Block-diagram of fuzzy logic controller of an F-DSTATCOM

3.3.1 Design of Fuzzy Logic Controller for D-STATCOM

The fuzzy logic controller is basically nonlinear and adaptive in nature, giving the robust performance in the cases wherein the effect of parameter variation of the controller is present. The inputs to the fuzzy controller are categorized as various linguistic variables with their
corresponding membership values. Seven labels are chosen for the linguistic variables to present the normalised input and output variables. These labels are PB (Positive Big), PM (Positive Medium), PS (Positive Small), Z (Zero), NS (Negative Small), NM (Negative Medium) and NB (Negative Big).

The load voltage deviation, $\Delta V(k)$ and its derivative, $\dot{\Delta} V(k)$ computed at an instant $k$ are normalized before fuzzification so that they vary from -1 to +1. The normalization is carried out by dividing $\Delta V(k)$ and $\dot{\Delta} V(k)$ by the respective maximum value. The maximum values of voltage deviation and its derivative are estimated from the simulation of the given test system without D-STATCOM for different disturbances. The output variable, $\Delta \delta(k)$ after defuzzification is in normalized form. This is then de-normalized to get the required output.

Linear triangular membership function as shown in Figure 3.14 is used in the design of FD-STATCOM. $\mu(e)$, $\mu(ce)$ and $\mu(\delta)$ are the membership function associated with the linguistic variables error ($e$), change in error ($ce$) and output ($\delta$) respectively. The width is chosen to be equal for all the labels of each one of the two input variables in order to keep the number of parameters to be optimized a minimum. The widths of the labels are $W_{L1}$ and $W_{L2}$ for $\Delta V(k)$ and $\dot{\Delta} V(k)$ respectively. The width of all the labels of output variable is chosen to be the same and it is set to 0.666. For a given pair of input variable $\Delta V(k)$, $\dot{\Delta} V(k)$ the output variable $\Delta \delta(k)$ is computed as detailed below.
The normalised input variables $\Delta V(k)$ and $\dot{\Delta} V(k)$ are first fuzzified, i.e. the numerical values are converted to the seven linguistic labels with appropriate membership value. With two input variable and each variable having seven labels there will be 49 input label pairs. A rule table relating each one of the 49 input label pairs to the respective output label is given in Table 3.2 (Driankov et al 2001).

**Table 3.2 Rule table for FD-STATCOM output**

<table>
<thead>
<tr>
<th>$ce$</th>
<th>NB</th>
<th>NM</th>
<th>NS</th>
<th>Z</th>
<th>PS</th>
<th>PM</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NM</td>
<td>NS</td>
<td>Z</td>
</tr>
<tr>
<td>NM</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NM</td>
<td>NS</td>
<td>Z</td>
<td>PS</td>
</tr>
<tr>
<td>NS</td>
<td>NB</td>
<td>NB</td>
<td>NM</td>
<td>NS</td>
<td>Z</td>
<td>PS</td>
<td>PM</td>
</tr>
<tr>
<td>Z</td>
<td>NB</td>
<td>NM</td>
<td>NS</td>
<td>Z</td>
<td>PS</td>
<td>PM</td>
<td>PB</td>
</tr>
<tr>
<td>PS</td>
<td>NM</td>
<td>NS</td>
<td>Z</td>
<td>PS</td>
<td>PM</td>
<td>PB</td>
<td>PB</td>
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<td>PM</td>
<td>NS</td>
<td>Z</td>
<td>PS</td>
<td>PM</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
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<td>Z</td>
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<td>PM</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
</tr>
</tbody>
</table>
Consider a typical rule:

If \((\Delta V(k) \text{ is } \text{PB} \text{ AND } \dot{\Delta} V(k) \text{ is } \text{PM})\) THEN \(\Delta \delta(k)\) is PB. When this rule is fired, the membership function of the two input variables is compared. The minimum of the two is obtained and assigned as the value of the output linguistic variable membership function (PB).

Let the membership functions of \(\Delta V(k)\) (when it is PB) and \(\dot{\Delta} V(k)\) (when it is PM) are \(\mu(e)\) and \(\mu(ce)\) respectively. The membership function \(\mu(\delta)\) of the output linguistic variable label, PB is given by:

\[
\mu(\delta) = \text{Min} \{\mu(e), \mu(ce)\} \tag{3.4}
\]

The last stage of the fuzzy logic control process is the defuzzification. It is the process of converting the fuzzy values into the crisp values. This process depends on the output fuzzy set, which is generated from the fired rules. Centroid method is used for defuzzification. Using the correlation product, output fuzzy set is formed. The crisp value of the output is determined by using the following equation:

\[
\Delta \delta(k) = \sum_{i=1}^{N} \left[ \frac{\mu(y_i) \ast y_i}{\sum_{i=1}^{N} \mu(y_i)} \right] \tag{3.5}
\]

where \(N = \text{number of rules fired}, \ y_i = \text{value of the normalised output label which is taken as the midpoint of the width of the label}, \ \mu(y_i) = \text{membership function of the normalised output assigned using Equation (3.1)}\) and
defuzzified change in controller output. The output is then

denormalized to get the required output.

3.3.2 PSCAD/EMTDC Simulation Results

The investigations are carried out on the 230 kV/11 kV test system
whose specifications are already discussed in section 3.2.3. The simulation
results without D-STATCOM for the load scenario of voltage sag from
(0.3 to 0.6) sec and swell from (0.9 to 1.2) sec is shown in Figure 3.3 of
section 3.2.3. The overshoots in the RMS voltage due to the control action of
CD-STATCOM as shown in Figure 3.15 is greatly reduced by employing
FD-STATCOM, as shown in Figure 3.16(a). It is observed that the
FD-STATCOM yields smooth control of RMS voltage at the PCC. The
system response with FD-STATCOM settles to the steady state very quickly
in comparison with the system response using CD-STATCOM. The
FD-STATCOM results are better to those obtained with the CD-STATCOM
for every load perturbation. Figure 3.16(b) to (c) is the blown up picture of
Figure 3.16(a).

3.3.2.1 Investigation of robustness

The performance of FD-STATCOM has been evaluated for a wide
range of operating conditions and it is observed to be robust and work
satisfactorily for sudden network impedance variations by ± 30 % resulting in
to voltage sag and voltage swell. However, in CD-STATCOM the $K_p$ and $K_i$
settings has to be changed for wide load variations.
Figure 3.15 RMS voltage at PCC with CD-STATCOM

Figure 3.16 (a) RMS voltage at PCC with FD-STATCOM (b) Zoomed version of the RMS voltage during voltage sag (c) Zoomed version of the RMS voltage during voltage swell
3.4 FUZZY LOGIC BASED ACTIVE POWER LINE CONDITIONER

Active Power Line Conditioner (APLC) also called as Active Power Filter (APF) is used for compensating reactive power and harmonics in distribution system. They also have additional functions such as compensation for current and voltage unbalance, voltage flicker, voltage sag and swell mitigation. The voltage related compensations (voltage harmonics, voltage unbalance, voltage sag, flicker, etc.) are carried out using series APLC’s, while current related compensations (reactive power, current unbalance, etc.) are made using shunt APLC’s.

Current control techniques (Buso et al 1998) such as linear current control, hysteresis control, deadbeat control, etc., are available to obtain the control signals for the switching devices of the APLC. Although hysteresis control is simple and robust, it produces a varying modulation frequency for the power converter causing Electro-Magnetic Interference (EMI) problems. The deadbeat control strategy has the disadvantage of being sensitive to the parametric variation of the control system. But the nonlinear control technique, such as Sliding Mode Control (SMC) provides a systematic approach to the problem of maintaining stability and performance in the presence of modeling uncertainty (Saetieo et al 1995).

In line with this, the following investigations are carried out in this thesis. A nonlinear, single-phase and three-phase fuzzy sliding mode controller based APLC has been designed and presented with simulation results. An improvement over conventional linear control is achieved with this nonlinear control law, which overcomes the bandwidth limitations.
3.4.1 Single-Phase Active Power Line Conditioner

This work is motivated by systems which contain multiple nonlinear loads, whether they may be uncontrolled rectifiers for DC based loads, triac based controllers for heating applications or some combination of the above. These loads draw currents with high harmonic content and poor power factor. The use of APLC for compensating harmonic distortion and reactive power in the electrical networks, both at user level or at higher voltage level is preferred than the classical passive compensating methods. APLC permits the control and the compensation of the distorted line currents adapting themselves to the load changes and to changing in working frequency (Torrey 1995). The load used in this work is an uncontrolled rectifier in parallel with an AC controller as shown in the Figure 3.17.

![Figure 3.17 Single-phase shunt APLC with nonlinear loads](image-url)
The APLC used to compensate for these two nonlinear loads is a single-phase inverter. The shunt APLC is controlled by a Proportional-Integral (PI) controller and Fuzzy Controller (FC) using Sliding Mode Control (SMC) concept. They are used to shape the line current to be in phase and of the same shape as the supply voltage. This configuration is simulated using MATLAB/SIMULINK. The effect of single-phase APLC on line current harmonic reduction and power factor correction is presented.

The SMC concepts including inverter model for the APLC, which addresses the design of the controller are discussed in the forthcoming section.

3.4.1.1 The inverter model

The inverter used as an APLC is shown in Figure 3.18. The switches shown support unipolar voltage, bipolar current and are operated in a manner which forces the inductor current \(i_L\), to follow whatever shape that is necessary such that the total load current drawn by the filter and nonlinear loads is of the correct magnitude and of the same shape as the input voltage. The nominal capacitor voltage must be larger than the peak of the AC source. This enables \(i_L\) to be shaped as required at any point in the supply cycle.

Assume \(\nu_c > |\nu_s|\). During the positive half cycle of the source voltage, \(i_L\) is made more positive by making \(\nu_x = 0\). It is driven towards zero by making \(\nu_x = \nu_c\). During the negative half cycle of the source voltage, \(i_L\) is made more negative by making \(\nu_x = 0\); and is driven towards zero by making \(\nu_x = -\nu_c\). It is concluded that the two switches in each leg of the inverter are used for different tasks. The switches \(S_3\) and \(S_4\) are used to force
\( \nu_x \leq 0 \) and \( \nu_x \geq 0 \) respectively, while the switches \( S_1 \) and \( S_2 \) actively shape, \( i_L \) (Kassakian 1991).

\[ u_x = \begin{cases} 1 & \text{when } S_x \text{ is conducting} \\ 0 & \text{when } S_x \text{ is open} \end{cases} \]

where \( x \) denotes the switch number. The two switches in each inverter leg must operate in a complementary fashion.

This gives

\[ u_1 + u_2 = 1 \]  \hspace{1cm} (3.6)

and

\[ u_3 + u_4 = 1 \]  \hspace{1cm} (3.7)
The definition of $u$ for each switch, $u_x$, is written in terms of capacitor voltage ($u_c$) as,

$$u_x = (u_1 u_4 - u_2 u_3) u_c$$  \hspace{1cm} (3.8)

By combining (3.6) and (3.7) $u_x$ is also written as,

$$u_x = (u_1 + u_4 - 1) u_c$$  \hspace{1cm} (3.9)

Further,

$$i_c = (u_1 + u_4 - 1) i_L$$  \hspace{1cm} (3.10)

From (3.9) and (3.10) the state equations for the inductor current and capacitor voltage are written as,

$$\frac{di_L}{dt} = \frac{1}{L} \left[ u_s - (u_1 + u_4 - 1) u_c \right]$$  \hspace{1cm} (3.11)

$$\frac{du_c}{dt} = \frac{1}{C} \left[ (u_1 + u_4 - 1) i_L \right]$$  \hspace{1cm} (3.12)

### 3.4.1.2 Sliding mode control

SMC is concerned with forcing one or more variables to follow a specific trajectory (Slotine et al 1983). The trajectory is known as the sliding surface. The nonlinear control law is chosen such that regardless of where the system variables are, the control action always drives the system to the sliding surface. The source current is forced to be in phase and same shape as the supply voltage for the APLC applications.
A sliding surface is proposed and the trajectory for line current is given by,

\[ i_s^* = k u_s \quad (3.13) \]

where \( k \) is a scaling factor based on real power demand of the load. The standard form for sliding surface \( (S) \) is given as,

\[ S = i_s - k u_s = 0 \quad (3.14) \]
\[ S = i_s - i_s^* = 0 \quad (3.15) \]

To assure that the system is maintained on the sliding surface, it is shown that there is a natural control, which satisfies

\[ \frac{dS}{dt} \leq 0 \quad (3.16) \]

for all values of the line current. If it is not satisfied then the desired trajectory cannot be maintained.

The equation (3.16) is also satisfied by controlling the sign on \( \frac{di_s}{dt} \).

At any point in time, the filter forces \( \frac{di_s}{dt} \) to be positive or negative through proper operation of the switches. In addition, proper design of the power circuit ensures that \( \frac{di_s}{dt} \) is greater than \( k \frac{du_s}{dt} \). The nonlinear control law used to implement the SMC law for the shunt APLC is given in Table 3.3.
3.4.1.3 Design of the controller scheme for single-phase shunt APLC

In the open loop, the switches $S_3$ and $S_4$ (Figure 3.18) are operated at 50 Hz and switches $S_1$ and $S_2$ (Figure 3.18) are operated at 50 kHz. In this case, the current injected by the filter is independent of distorted source current. The source current of the single-phase system supplying the multiple nonlinear loads is not a pure sine wave. In order to shape the source current to be sinusoidal, a closed loop control is necessary. In the closed loop control, the actual source current and the sinusoidal reference current are compared and switching pulses for switches $S_1$ and $S_2$ are produced. The closed loop controller for shunt APLC is shown in Figure 3.19. It has an inner current control loop and an outer voltage control loop. The inner current control loop uses SMC law to shape the line current. The outer voltage loop decides the magnitude of the reference line current ($k$). During start-up of the APLC, the control signals to the active switches are disabled for one-half line cycle. This provides adequate time for the capacitor to charge through the uncontrolled rectifier formed by the diodes in anti-parallel with each controllable switch. By virtue of the inductance ($L_f$) on the AC side of the active filter, the capacitor voltage charges to a value in excess of the peak of the AC source voltage. This provides adequate voltage for the APLC to begin operation.

<table>
<thead>
<tr>
<th></th>
<th>$i_s &lt; k\nu_s$</th>
<th>$i_s &gt; k\nu_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$S_2$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$S_3$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$S_4$</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
The capacitor voltage is given to a low pass filter, which gives average capacitor voltage. This \( v_c \) is compared with nominal set point capacitor voltage. The error is processed using conventional PI and Fuzzy Controller (FC). The output of the controller is the proportionality factor \( k \). The reference line current, \( i_{\text{line}}^* \) is obtained through multiplication of \( k \) with \( u_s \). The reference line current is compared with the actual source current. This is given to the input of D flip flop. The output of the D flip flop is given to switches \( S_1 \) and \( S_2 \) (Figure 3.19). The gating pulses for the switches \( S_3 \) and \( S_4 \) (Figure 3.19) are derived based on the supply voltage. For \( u_s > 0 \), switch \( S_4 \) is ON and \( u_s < 0 \) switch \( S_3 \) is ON.

### 3.4.1.4 Fuzzy controller

The nonlinear load variation, changes in capacitor voltage and inductor current affect the source current. The harmonics present in the source current are compensated by developing a suitable switching pattern for the APLC. The shunt APLC controlled using PI controller is reported in (Torrey 1995). Accordingly, PI controller is developed and simulated. The control of the distortions by proper switching is first simulated by the conventional PI controller for a particular operating condition. The PI controller settings are found to work satisfactorily only for a particular loading condition. When the conventional PI controller is employed the source current shaping is achieved along with the significant amount of spikes. The error due to the switching action of the inverter leads to this high frequency ripple component of the source current.
A mamdani type fuzzy logic controller is proposed for multiple nonlinear loads to limit the line current distortion using single-phase APLC. In the presence of FC, the source current shaping is achieved with negligible amount of spikes resulting in reduction in THD. The time taken by the conventional PI controller in shaping the line current is 0.12 sec whereas with FC it takes 0.06 sec. Thus, the proposed FC has better dynamic behavior than conventional PI control. It is claimed that the fuzzy logic control yields the results, which are superior to those, obtained with the conventional controller reported earlier by (Torrey, 1995). In the FC, the simplicity of a PI controller is combined with the intelligence and adaptiveness of the fuzzy logic based control system. Therefore, the FC is characterized as an intelligent-adaptive controller.

The two input signals for the proposed FC are capacitor voltage error (e) and change in error (ce), which is properly scaled and fuzzified. Five membership functions are used for error; change in error and also for controller output (k). Linear triangular membership function is used in the
design of FC for shunt APLC. With two input variables and each variable having five labels there will be 25 input label pairs. A rule table relating each one of the 25 input label pairs to the respective output label is given in Table 3.4. The defuzzyfication stage produces the final crisp value of k. The centroid method is employed for defuzzyfication.

<table>
<thead>
<tr>
<th>Table 3.4  Rule Table for APLC Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>NB</td>
</tr>
<tr>
<td>NS</td>
</tr>
<tr>
<td>Z</td>
</tr>
<tr>
<td>PS</td>
</tr>
<tr>
<td>PB</td>
</tr>
</tbody>
</table>

3.4.1.5 Simulation results

The single-phase PI controller and FC based APLC are modeled and simulated using MATLAB/SIMULINK. The uncontrolled rectifier load together with the Triac based AC voltage controller is considered as multiple nonlinear loads. The simulation system parameters are given in Table 3.5. The Figures (3.20 to 3.22) document the performance of the system shown in Figure 3.17 for one steady-state operating point.
Table 3.5  Simulation system parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>System voltage</td>
<td>120 V&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>System frequency f = 50 Hz</td>
<td></td>
</tr>
<tr>
<td>Uncontrolled rectifier</td>
<td>R = 37.5Ω , C = 1200 µf</td>
</tr>
<tr>
<td>AC voltage controller</td>
<td>R = 25Ω, firing angle (α) = 36°</td>
</tr>
<tr>
<td>Shunt APLC</td>
<td>AC filter capacitor (C&lt;sub&gt;f&lt;/sub&gt;) = 1300 µf</td>
</tr>
<tr>
<td></td>
<td>AC filter inductor (L&lt;sub&gt;f&lt;/sub&gt;) = 1.88 mH</td>
</tr>
<tr>
<td>PI controller</td>
<td>K&lt;sub&gt;p&lt;/sub&gt; = 0.022; K&lt;sub&gt;i&lt;/sub&gt; = 1.0</td>
</tr>
<tr>
<td>LPF</td>
<td>Bandwidth=90 Hz and decision frequency (f&lt;sub&gt;d&lt;/sub&gt;) =50 kHz</td>
</tr>
</tbody>
</table>

The source voltage of the test system is given in Figure 3.20. The load current before compensation, compensated source current using FC based APLC, compensated source current using PI controller based APLC, the filter current using FC and PI controller based APLC are given in Figure 3.21(a) to (e) respectively. The sum of filter current and load current gives the source current. These results confirm that the source current is of the same shape as the source voltage and in phase with it. The commands to switches S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub> and S<sub>4</sub> are shown in Figure 3.22(a) to (d) respectively. These waveforms are consistent with Table 3.3.

The performance of fuzzy based APLC has been evaluated for a wide range of operating conditions and it is observed to be robust and work satisfactorily for sudden load power variations of the network by ± 15 %. However, in PI controller based APLC the K<sub>p</sub> and K<sub>i</sub> settings has to be changed for load power variations. The simulation results of percentage current THD and power factor before and after the implementation of PI and fuzzy based APLC are shown in Table 3.6.
Figure 3.20 Source Voltage

(a) Load current (A)
(b) Source Current (A)
(c) Source Current (A)
Figure 3.21 Performance of shunt APLC  (a) Load current before compensation (b) Compensated source current using fuzzy based APLC (c) Compensated source current using PI based APLC (d) Filter current using fuzzy based APLC (e) Filter current using PI based APLC
The percentage THD measured in the presence of fuzzy based APLC are within the IEEE 519 harmonic standards. The power factor of the system gets improved. The fuzzy control demonstrates better dynamic behaviour than conventional PI control. The main advantages of this approach are the inverter system operates simultaneously as an active filter compensating for the harmonics and as a power factor compensator.
3.4.2 Three-Phase Active Power Line Conditioner (Sharmeela et al 2007)

This section presents the analysis, design and operation of three-phase shunt APLC to compensate for the nonlinearity in the phase-controlled converter. The nonlinear load used in this proposed work is a controlled rectifier as shown in the Figure 3.23.

The APLC comprises of six-switch three-phase inverter, a DC bus capacitor and an isolation transformer. The leakage inductance associated with each phase of the isolation transformer is used as the series impedance with each phase, by which the APLC actively shape the phase currents. The inverter is controlled using two controllers. A fast inner loop is used to control the shape of the line currents, forcing them to be of the same shape, and in phase with, the phase voltages. The inner current regulation loop is based on SMC which is simple and very easy to implement. The outer voltage control loop uses the PI controller/ FC to regulate the average voltage on the DC bus capacitor. The outer voltage loop is used to set the proper magnitude of the phase currents (Saetieo, 1995). The single-phase APLC control and working principle discussed in section 3.4.1 is extended to the three-phase shunt APLC.

The PI based APLC works satisfactorily only for continuous current mode. It fails to operate satisfactorily for discontinuous current mode. The FC based APLC has better dynamic behaviour than conventional PI controller based APLC. It compensates better for both continuous and discontinuous modes of operation.
3.4.2.1 Design of the controller scheme for three-phase APLC

In the open loop, the switches $S_1$ - $S_6$ (Figure 3.23) are operated at $180^\circ$ mode of conduction for the three-phase VSI. In this case, the current injected by the filter is independent of distorted source current. The source current of the three-phase system supplying the controlled rectifier load is not a pure sine wave. In order to shape the source current to be sinusoidal, a closed loop control is necessary. In the closed loop control, the actual source current and the sinusoidal reference current are compared and switching pulses for switches $S_1$ - $S_6$ (Figure 3.23) are produced.
The closed loop controller for three-phase APLC is shown in Figure 3.24. It has an inner current control loop and an outer voltage control loop. The inner current control loop uses SMC law to shape the line current. The outer voltage loop decides the magnitude of the reference line current (k). During start-up of the APLC, the control signals to the active switches are disabled for one-half line cycle. This provides adequate time for the capacitor to charge through the uncontrolled rectifier formed by the diodes in anti-parallel with each controllable switch. By virtue of the inductance (Lc) on the AC side of the active filter, the capacitor voltage charges to a value in excess of the peak of the AC source voltage. This provides adequate voltage for the APLC to begin operation.

The capacitor voltage is given to a low pass filter, which gives average capacitor voltage. This \( v_c \) is compared with nominal set point capacitor voltage. The error is processed using conventional PI and FC. The output of the controller is the proportionality factor (k). The reference line current, \( i_{\text{line}}^* \) is obtained through multiplication of k with \( v_c \). The reference line current is compared with the actual source current. This is given to the
input of the SMC. The output of the SMC is given to switches $S_1$ - $S_6$
Figure 3.24.

### 3.4.2.2 Fuzzy controller

The two input signals for the proposed FC are capacitor voltage error ($e$) and change in error ($ce$) which is properly scaled and fuzzified. Five membership functions are used for error; change in error and also for controller output $k$. Linear triangular membership function is used in the design of FC for three-phase APLC. With two input variable and each variable having five labels there will be 25 input label pairs. A rule table relating each one of the 25 input label pairs to the respective output label is given in section 3.4.1.4 (Table 3.4). The defuzzification stage produces the final crisp value of $k$. The centroid method is employed for defuzzification.

The nonlinear load variation, changes in capacitor voltage and inductor current affect the source current. The harmonics present in the source current are compensated by developing a suitable switching pattern for the APLC. The three-phase APLC controlled using PI controller is reported in (Saetieo, 1995). Accordingly, PI controller is developed and simulated. The control of the distortions by proper switching is first simulated by the conventional PI controller for a particular operating condition. The PI controller settings are found to work satisfactorily only for the continuous mode of operation. When the conventional PI controller is employed the source current shaping is achieved along with the significant amount of spikes. The error due to the switching action of the inverter leads to this high frequency ripple component in the source current.

The PI controller setting fails to correct the source current for the discontinuous mode of the nonlinear load. Therefore, a mamdani type fuzzy logic controller is proposed to limit the line current distortion using
three-phase APLC. In the presence of FC the source current shaping is achieved with negligible amount of spikes resulting in percentage reduction in THD. The time taken by the conventional PI controller in shaping the line current during continuous mode is 0.1 sec whereas with fuzzy controller it takes 0.08 sec. Even though the output waveforms of both PI and FC for shunt APLC looks similar, FC has better dynamic behaviour compared to PI controller.

The fuzzy based APLC gives a better compensation for the source current during the discontinuous mode of conduction than the PI control based APLC. This is because of the inherent robustness in the fuzzy based APLC which does not require parameter re-tuning. The PI controller gives the fast response only if proportional and integral constants are tuned adaptively on the occurrence of load disturbances. Thus, the fuzzy controller works satisfactorily for both continuous and discontinuous mode of operation with the nonlinear load. It is claimed that the fuzzy logic control yields the results, which are superior to those obtained with the conventional PI controller reported earlier by Saetieo (1995).

### 3.4.2.3 Simulation results

The simulation system parameters for the three-phase APLC are given as follows. Supply = 120 V\(_{\text{rms}}\), \(f = 50\) Hz, Coupling transformer = 3:1, Controlled rectifier load with \(R = 6\) Ω, \(L = 26.5\) mH. The filter capacitor = 1300 μF and filter inductor = 1.88 mH. The firing angle (α) for the controlled rectifier load is set at \(\alpha = 0^\circ\) (Continuous) and \(\alpha = 90^\circ\) (discontinuous). The bandwidth of the low pass filter is 90 Hz and \(f_d\) (decision frequency) = 32 kHz. The \(K_p = 0.022\) and \(K_i = 1.0\) are chosen for the PI controller. The simulations for the three-phase shunt APLC are performed using MATLAB/SIMULINK. However, the simulation results for the phase-A of PI
and fuzzy based three-phase shunt APLC are presented here. The percentage current THD of PI and fuzzy based shunt APLC for continuous mode and discontinuous mode of operation are shown in Table 3.7. The percentage current THD measured verifies the significant reduction in current harmonics by using PI and fuzzy based shunt APLC. However, the percentage current THD measured in the presence of fuzzy based APLC are within the IEEE 519 harmonic standards.

Table 3.7 Comparison of percentage current THD in continuous and discontinuous modes

<table>
<thead>
<tr>
<th>Modes of Operation</th>
<th>Percentage Current THD of Phase-A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without APLC</td>
</tr>
<tr>
<td>Continuous mode</td>
<td>38.84</td>
</tr>
<tr>
<td>Discontinuous mode</td>
<td>57.51</td>
</tr>
</tbody>
</table>

The supply voltage of the test system is given in Figure 3.25. The source current before compensation for the continuous mode is given in Figure 3.26. The compensated source current for continuous mode using PI and Fuzzy controller are given in Figures 3.27 and 3.28 respectively. The source current before compensation for the discontinuous mode is given in Figure 3.29. The compensated source current for discontinuous mode using PI and Fuzzy controller are given in Figures 3.30 and 3.31 respectively.

Figure 3.25 Supply voltage of Phase-A
Figure 3.26 Source current (Continuous Mode) of Phase-A before compensation

Figure 3.27 Compensated source current (Continuous Mode) of Phase-A using PI controller

Figure 3.28 Compensated source current (Continuous Mode) of Phase-A using fuzzy controller

Figure 3.29 Source current (Discontinuous Mode) of Phase-A before compensation
3.5 WAVELET TRANSFORM BASED CONTROL FOR SINGLE-PHASE ACTIVE POWER LINE CONDITIONER

The increasing use of power-electronics based loads to improve the system efficiency and controllability is increasing the concern for harmonic distortion levels in end use facilities and overall power system. The presence of harmonics in the power lines results in greater power losses in distribution system, interference problem in communication system and also in operation failure of electronics equipment. Traditional solutions use capacitor and inductor to makeup a passive filter for current harmonics elimination and power factor improvement. Passive filter ratings have to be coordinated with reactive power requirements of the loads and it is often difficult to design
these filters to avoid leading power factor operation during light load conditions. The large passive component, fixed compensation characteristics, series and parallel resonance are the main drawbacks of passive filter. APLC overcomes the drawbacks of passive filter. They are considered as effective and practical solutions for the increasing problems of power quality.

Shunt APLC has been recognized as an effective and practical solution to current harmonic and reactive power compensation of nonlinear loads. The basic principle of shunt APLC is that it generates a current equal, opposite on polarity to the harmonic current drawn by the load and injects it to the PCC thereby forcing the source current to be pure sinusoidal. As a consequence, the characteristics of the harmonic compensation are strongly dependent on the filtering algorithm employed for the calculation of load current harmonics.

There are different techniques proposed (Grady et al (1990), Marques et al (1998) in the literature based on different theories to calculate the compensation reference current template. The effectiveness of these algorithms varies according to the assumptions made during the development of the theory. The fundamental issue for shunt APLC design is the selection of a compensation strategy, that is, the procedure for evaluating the compensating reference current. In this thesis work, the application of the Wavelet Transform-Multi Resolution Analysis (WT-MRA) is presented and is found to be most suitable for extracting the compensating reference signal in order to control the mitigation devices such as APLC (Driesen 2002). A new control algorithm employing Discrete Wavelet Transform (DWT) for shunt APLC is proposed to compensate for the line current harmonics. The role of the DWT here is to detect the frequency content present in the distorted signal and extract the reference signal which is used to drive the sliding mode controller of APLC.
Figure 3.32 shows the schematic diagram of WT based control for single-phase APLC. The uncontrolled rectifier load together with the Triac based AC voltage controller is considered as multiple nonlinear loads. It distorts the source current. The implementation of current regulators is realized by single-phase VSI with capacitive energy storage at the DC side. The inverter switches are operated in a manner which forces the inductor current ($i_L$), to follow whatever shape is necessary such that the total load current drawn by the filter and the nonlinear loads is of the correct magnitude and of the same shape as the input voltage. Initially, the capacitor is charged through the uncontrolled rectifier formed by the diode in anti-parallel with each controllable switch.

The modeling of inverter and the switching operation of the inverter using the sliding mode controller for single-phase shunt APLC discussed in section 3.4.1 is extended to the WT based control for single-phase shunt APLC. WT uses variable window sizes to determine the frequency content present in the distorted signal and extract the reference current which is used to drive the APLC for harmonic compensation. The gating pulses for the single-phase inverter are generated based on the harmonic content present in the source.
Figure 3.32  Schematic diagram of WT based control for single-phase APLC

3.5.1   Design of the WT based Controller Scheme for Single-Phase Shunt APLC

In the open loop, the switches $S_3$ and $S_4$ (Figure 3.32) are operated at 50 Hz and switches $S_1$ and $S_2$ (Figure 3.32) are operated at 50 kHz. In this
case, the current injected by the filter is independent of distorted source current. The source current of the single-phase system supplying a nonlinear load is not a pure sine wave. In order to shape the source current to be sinusoidal, a closed loop control is necessary. In the closed loop control, the actual source current and the sinusoidal reference current extracted from the distorted source current using WT are compared and switching pulses for switches $S_1$ and $S_2$ are produced. The closed loop controller for shunt APLC is shown in Figure 3.32. It has a current control loop which extracts reference current using wavelet and uses SMC law to shape the line current. The voltage loop decides the magnitude of the phase currents. During start-up of the APLC, the control signals to the active switches are disabled for one-half line cycle. This provides adequate time for the capacitor to charge through the uncontrolled rectifier formed by the diodes in anti-parallel with each controllable switch. By virtue of the inductance ($L_d$) on the AC side of the active filter, the capacitor voltage charges to a value in excess of the peak of the AC source voltage. This provides adequate voltage for the APLC to begin operation.

The extracted reference line current $i_{\text{line}}^*$ is compared with the actual source current and given to D flip flop. The output of the D flip flop is given to switches $S_1$ and $S_2$. The gating pulses for the switches $S_3$ and $S_4$ are derived based on the supply voltage. For $\upsilon_s > 0$, switch $S_4$ is ON and $\upsilon_s < 0$ switch $S_3$ is ON.

3.5.2 Reference Current Extraction using DWT

The de-noising property of the DWT has been utilized to determine the current reference signal for the APLC. The original signal is decomposed into high frequency and low frequency components. By reconstructing the signal after applying threshold, the higher frequency components are
eliminated and a signal devoid of high frequency contents is extracted. This signal is used as the reference signal for the sliding mode controller. The distorted signal is sampled at a certain sampling frequency and the number of levels to which the signal has to be decomposed depends on the sampling frequency. At each level of decomposition the frequency content of the sampled signal is divided into half and the lower frequency content is retained to extract the reference template.

The principle of the DWT lies in the hierarchical composition of an input signal into a series of successively lower resolution signals, providing an effective way of looking at a signal at various scales and analyzing it with various resolutions. The non-stationary signal is effectively analyzed using WT. It gives the required resolution by automatically adjusting the window function. It allocates greater resolution in time for the high frequency component of a signal and greater resolution in frequency for low frequency component of a signal. Both time and frequency information of signal is obtained and the frequency component of the given signal is also separated through this technique.

In the proposed work, Meyer wavelet is used because it accurately picks up the non-continuative point of the frequency components. WT is implemented using a tree-structured filter bank. Figure 3.33 describes a two-band wavelet decomposition process to extract the reference current from the distorted source current. This process is also generalized to be n-band decomposition, where n is the number of frequency bands in which the decomposed signals are situated. The process starts with a low-pass filter \( H(n) \) and a high-pass filter \( G(n) \) that decomposes the original signal (i.e., distorted source current) into \( S_1(n) \) and \( D_1(n) \). Then, the post filtered signal
108

Figure 3.33 Wavelet Decomposition Process

$S_1(n)$ is further decomposed into $S_2(n)$ and $D_2(n)$ through the digital filter $G(n)$ and $H(n)$. In the block diagram of Figure 3.33, the signal $S_1(n)$ is seen computed from the convolution of $G(n)$ with original signal coefficient plus a down-sampling with a factor of two, while $D_1(n)$ is obtained from the convolution of original signal with $H(n)$ plus a down sampling with a factor of two. With this operation, the signal $S_1(n)$ contains lower frequency components and $D_1(n)$ contains higher frequency components. This process is called wavelet decomposition.

Wavelet reconstruction process is just reverse of the wavelet decomposition. The coefficient $S_2(n)$ is reconstructed as a signal by thresholding the coefficient $D_2(n)$, $D_1(n)$ and convoluting with $G(n)$ plus up sample by two, to get the signal $S_2$ (i.e., extracted reference current signal).
3.5.3 Simulation Results

The uncontrolled rectifier load together with the Triac based heating load is considered as multiple nonlinear loads. The simulation system parameters are shown in Table 3.8. The simulation results to validate the performance of WT based shunt APLC for harmonic current mitigation are shown in Figures 3.34(a) to (e). The source current before compensation and the source voltage are shown in Figure 3.34(a) and 3.34(b) respectively. The compensated source current and the filter current are shown in Figure 3.34(c) and 3.34(d) respectively. The reference current is extracted from the distorted source current using WT and is shown in Figure 3.34(e). The harmonic spectrum of source current before and after compensation are shown in Figure 3.35(a) and (b) respectively. The uncompensated source current contains 3, 5, 7 and 9 harmonics order. The source current after compensation contains only the fundamental component.

A new control method has been proposed for the shunt APLC. The proposed method is simple, easy to implement and insensitivity to voltage distortion. From the simulation results, it is seen that there is a significant reduction in harmonic distortion.

Table 3.8 Simulation system parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Voltage</td>
<td>60 V\text{ rms}</td>
</tr>
<tr>
<td>System Frequency</td>
<td>f = 50 Hz</td>
</tr>
<tr>
<td>Uncontrolled Rectifier</td>
<td>R = 210 Ω, C = 470 μf</td>
</tr>
<tr>
<td>AC Voltage Controller</td>
<td>R = 210 Ω, firing angle (α) = 30°</td>
</tr>
<tr>
<td>Shunt APLC</td>
<td>AC filter Capacitor, (C_f) = 720 μf</td>
</tr>
<tr>
<td></td>
<td>AC filter Inductor, (L_f) = 1.88 mH</td>
</tr>
</tbody>
</table>
Figure 3.34  Performance of WT based Shunt APLC (a) Source Current before compensation (b) Source voltage (c) Compensated source current (d) Filter current (e) Extracted reference current using WT
The concept of using Shunt Active Power Filter (SAPF) or Distribution Static Compensator (D-STATCOM) has been improvised to compensate for the harmonic currents caused by the locally connected nonlinear loads. This has been investigated and shown to be a viable solution for power quality improvement (Bhim Singh et al 1999). In general, linear and nonlinear control structures are used to analyze and control the SAPF. A constant switching frequency is achieved with Pulse Width Modulation (PWM) techniques based linear controllers. In using linear controller, a well-defined harmonics spectrum is obtained, but the properties of dynamics are limited. Compared to the use of linear controllers, the use of nonlinear ones based on hysteresis strategies allows faster dynamic response and better robustness. In hysteresis band control, the converter switching
actions are generated from the feedback control action through a hysteresis band around zero steady state error. The use of hysteresis controller results in high switching frequency and may be undesirable for second and higher order systems because the controller fails to stabilize the system error and the system enters into sustained oscillations (Ghosh et al 2002). The Sliding Mode Control (SMC) (Hung et al 1993 and Decarlo et al 1998) overcomes this drawback of hysteresis controller. The sliding mode switching function is one useful approach for stabilizing the second and higher order systems. Yet a large number of control strategies applied to SAPF have been reported, the SMC is robust and it seems to be the most appropriate one. This is because of the time-varying nature of SAPF making it suitable to be controlled by a variable structure approach such as the SMC (Mendalek et al 2002). The simplicity of the implementation makes the SMC particularly attractive.

In addition to the above mentioned features, the chattering caused by the switching operation, which is commonly considered a weakness of SMC. Nevertheless, with nonlinear controllers like SMC, the control is simple, easy to implement and the switching frequency of the controller is not constant. There are other controllers like Quasi-Sliding Mode Control (QSMC) with constant switching frequency (Moran et al 1995). In QSMC, the constant switching frequency is achieved by comparing the current error signal with a triangular reference waveform. The design of QSMC is as same as SMC technique.

Thus, a SAPF consists of Voltage Source Inverter (VSI), a reference current generation mechanism and a control mechanism for providing gating pulses to the VSI to track the reference current. In this chapter, the VSI is realized using three single-phase VSI fed by a common DC capacitor. This topology for VSI is selected and the two control techniques SMC and QSMC have been used for the control of SAPF. In this
proposed work, a method based on the theory of instantaneous symmetrical components (Ghosh et al 2000) is utilized as it has less computation. The aim of the proposed work is to compare the performances achieved by two simple and robust control techniques for SAPF, namely Sliding Mode Control (SMC also known as variable frequency type control) and Quasi Sliding Mode Control (QSMC also known as constant switching frequency type control).

3.6.1 System Description

The SAPF consists of three main parts namely active filter inverter, reference current generation technique and control technique. Figure 3.36 shows the general block diagram of SAPF.

Figure 3.36 General block diagram of shunt active power filter
3.6.1.1 Shunt active power filter inverter

The VSI used for the active filter is able to supply for both the balanced and unbalanced loads. The three-phase VSI cannot be used to supply for unbalanced loads because there is no path for the neutral currents to flow. Hence, in the proposed work the VSI for the active filter is made up of three-single phase VSI fed by a common DC capacitor, which are used to supply for both balanced and unbalanced loads. It is preferred over other inverter topologies used for unbalanced loads because of the following three main advantages. The capacitor voltage control is easier, independent control of each phase and less complex switching circuit.

Figure 3.37 shows the three single-phase VSI used for the shunt active power filter. \( S_1, S_2, S_3, S_4, S_5 \) and \( S_6 \) are power electronics switches like MOSFET, IGBT with anti-parallel diode. \( CP_1, CP_2 \) and \( CP_3 \) are coupling transformers used for the three phases. \( R_f \) and \( L_f \) are the filter resistance and filter inductance respectively. \( C_{dc} \) is the filter capacitor designed on the basis of the maximum DC ripple and the amount of the reactive power to be supplied. \( R_{Loss} \) represents the loss of DC capacitor.

![Diagram of three single-phase VSI for shunt active power filter]

Figure 3.37 Three single-phase VSI for shunt active power filter
3.6.1.1 Modeling of shunt active power filter inverter

Figure 3.38 shows the one arm of the three single-phase VSI used for the shunt active filter. The state equations describing the dynamics of the active filter are obtained by applying Kirchoff’s law at the PCC.

\[
\begin{align*}
    v_{dc} (S_1 - S_4) &= R_f i_{fa} + L_f \frac{di_{fa}}{dt} + v_{sa} \\
    v_{dc} (S_3 - S_6) &= R_f i_{fb} + L_f \frac{di_{fb}}{dt} + v_{sb} \\
    v_{dc} (S_5 - S_2) &= R_f i_{fc} + L_f \frac{di_{fc}}{dt} + v_{sc}
\end{align*}
\]

\[C_{dc} \frac{dv}{dt} = -(S_1 - S_4) i_{fa} - (S_3 - S_6) i_{fb} - (S_5 - S_2) i_{fc} + \frac{v_{dc}}{R_{Loss}}\] (3.17)

The variables \(i_{fa}, i_{fb}, i_{fc}, v_{dc}\) are the respective filter currents and DC capacitor voltage respectively. This model belongs to a class of multivariable nonlinear system. It is time invariant during a given switching state.
This model is represented in state space equation as

\[ X = AX + BU + C \]  \quad (3.18) \]

where

\[ X = \begin{bmatrix} X_1 & X_2 & X_3 & X_4 \end{bmatrix}^T = \begin{bmatrix} I_{fa} & I_{fb} & I_{fc} & V_{dc} \end{bmatrix}^T \]

\[ U = \begin{bmatrix} U_a & U_b & U_c \end{bmatrix}^T, \quad U_a = S_1 - S_4, \quad U_b = S_1 - S_3, \quad U_c = S_4 - S_2 \]

When upper switches are ON then \( S_1, S_3, S_5 = 1 \) and \( S_2, S_4, S_6 = 0 \) and when lower switches are ON then \( S_1, S_3, S_5 = 0 \) and \( S_2, S_4, S_6 = 1 \).

\[ A = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 & 0 \\ 0 & 0 & -\frac{R_f}{L_f} & 0 \\ 0 & 0 & 0 & -\frac{1}{R_{\text{loss}}C_{dc}} \end{bmatrix}, \quad B = \begin{bmatrix} X_4 & 0 & 0 \\ 0 & X_4 & 0 \\ 0 & 0 & X_4 \\ -X_1 & -X_2 & -X_3 \end{bmatrix} \]

\[ C = \begin{bmatrix} -\frac{V_{sa}}{L_f} \\ -\frac{V_{sb}}{L_f} \\ -\frac{V_{sc}}{L_f} \\ 0 \end{bmatrix} \]
3.6.1.2 Reference current generation

The reference currents for SAPF are generated using instantaneous symmetrical components theory. It does not require complex transformation of currents and voltages. It makes compensation for any kind of unbalance and harmonics in the load.

The objective is to provide balanced and sinusoidal supply current so that its zero sequence component is zero. It is given by

\[ i_{sa} + i_{sb} + i_{sc} = 0 \]  \hspace{1cm} (3.19)

The desired power factor is got by assuming that \( i_{sa1} \) lags or leads \( v_{sa1} \) by an angle \( \phi \) (i.e.)

\[ \angle v_{sa1} = \angle i_{sa1} + \phi \]  \hspace{1cm} (3.20)

\( v_{sa1} \) and \( i_{sa1} \) are obtained using symmetrical components theory.

\[
\begin{pmatrix}
  v_{sa0} \\
v_{sa1} \\
v_{sa2}
\end{pmatrix}
= \frac{1}{\sqrt{3}}
\begin{pmatrix}
  1 & 1 & 1 \\
  1 & a & a^2 \\
  1 & a^2 & a
\end{pmatrix}
\begin{pmatrix}
  v_{sa} \\
v_{sb} \\
v_{sc}
\end{pmatrix}
\hspace{1cm} (3.21)
\]

Thus,

\[ \angle v_{sa} + av_{sb} + a^2v_{sc} = \angle i_{sa} + ai_{sb} + a^2i_{sc} + \phi \]  \hspace{1cm} (3.22)

Substituting the values for \( a \) and \( a^2 \) in equation (3.22) to get
\[
\angle \left( v_{sa} - \frac{1}{2} v_{sb} - \frac{1}{2} v_{sc} \right) + \frac{j \sqrt{3}}{2} (v_{sb} - v_{sc}) = \angle \left( i_{sa} - \frac{1}{2} i_{sb} - \frac{1}{2} i_{sc} \right) \\
+ \frac{j \sqrt{3}}{2} (i_{sb} - i_{sc}) + \phi
\]

(3.23)

Solving this,

\[
\tan^{-1} \left( \frac{k_1}{k_2} \right) = \tan^{-1} \left( \frac{k_3}{k_4} \right) + \phi
\]

(3.24)

where

\[
k_1 = \frac{\sqrt{3}}{2} (v_{sa} - v_{sb}) \, , \, k_2 = \left( v_{sa} - \frac{1}{2} v_{sb} - \frac{1}{2} v_{sc} \right) \\
k_3 = \frac{\sqrt{3}}{2} (i_{sa} - i_{sb}) \, , \, k_4 = \left( i_{sa} - \frac{1}{2} i_{sb} - \frac{1}{2} i_{sc} \right)
\]

Taking tan on both sides

\[
\frac{k_1}{k_2} = \frac{k_3}{k_4} + \tan \phi
\]

(3.25)

Solving this to get

\[
(v_{sb} - v_{sc} - 3\beta v_{sa}) i_{sa} + (v_{sc} - v_{sa} - 3\beta v_{sb}) i_{sb} + (v_{sa} - v_{sb} - 3\beta v_{sc}) i_{sc} = 0
\]

(3.26)

where

\[
\beta = \frac{\tan \phi}{\sqrt{3}}
\]
When the power factor angle is assumed to be zero, equation (3.26) implies that the instantaneous reactive power supplied by the source is zero. On the other hand, when this angle is nonzero, the source supplies a reactive power that is equal to the instantaneous power. The instantaneous power in a balanced three-phase circuit is constant while for an unbalanced circuit it has a double frequency component in addition to the DC value. The objective of the compensator is to supply the double frequency component such that the source supplies the DC value of the load power. Therefore $p_{lav}$ is obtained.

$$p_{lav} = v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc}$$  (3.27)

$p_{lav}$ is computed using a Moving Average (MA) filter that has an averaging time of half cycle.

Combining Equations (3.19), (3.26) and (3.27)

$$\begin{bmatrix}
1 & 0 & 0 \\
v_{sb} & -v_{sc} & -3\beta v_{sa} \\
v_{sc} & v_{sa} - 3\beta v_{sb} & v_{sa} - v_{sb} - 3\beta v_{sc} \\
v_{sa} & v_{sb} & v_{sc}
\end{bmatrix} \begin{bmatrix}
i_{sa} \\
i_{sb} \\
i_{sc}
\end{bmatrix} = \begin{bmatrix} 0 \\
0 \\
p_{lav}
\end{bmatrix}$$  (3.28)

Assuming the currents are tracked without any error and applying KCL at PCC gives,

$$i_{fk}^* = i_{lk} - i_{sk}$$  (3.29)

where, $k = a, b, c$
Solving Equation (3.28) and substituting the values in Equation (3.29) gives the reference filter currents.

\[
\begin{align*}
\mathbf{i}_{fa}^* &= \mathbf{i}_{la} - \left( \frac{v_{sa} + (v_{sb} - v_{sc}) \beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \right) p_{lav} \\
\mathbf{i}_{fb}^* &= \mathbf{i}_{lb} - \left( \frac{v_{sb} + (v_{sc} - v_{sa}) \beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \right) p_{lav} \\
\mathbf{i}_{fc}^* &= \mathbf{i}_{lc} - \left( \frac{v_{sc} + (v_{sa} - v_{sb}) \beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \right) p_{lav} \tag{3.30}
\end{align*}
\]

Reference filter currents for all the phases are calculated by substituting all the values in the Equation (3.30). \( \beta \) is calculated for the desired power factor based on the required power factor angle \( \phi \) using \( \beta = \frac{\tan \phi}{\sqrt{3}} \).

### 3.6.1.3 Control techniques

This section discusses in detail about the two nonlinear controllers used for SAPF. They are namely Sliding Mode Control (SMC) also known as variable frequency type control and Quasi Sliding Mode Control (QSMC) also known as constant switching frequency type control.

#### 3.6.1.3.1 Sliding mode control

The active filter belongs to a class of time variant system. The control action of filter is discontinuous. The SAPF is considered to be a variable structure control system because periodic changes in the circuit
topology are performed to achieve the required compensation. In the proposed work, sliding mode control is used as it tracks the problem directly.

The main feature of the SMC is its insensitivity to system parameters once it reaches its sliding mode surface. Thus, SAPF is a natural candidate for sliding mode control. The general block diagram of SMC based SAPF is shown in Figure 3.39. The power rating of the SMC based SAPF is taken to be 20 kW. The SMC consists of three main design steps. The first step involves the defining of a sliding surface. The SMC existence has to be verified and the third step involves the analysis of stability into sliding surface.

Figure 3.39 Block diagram of SMC based SAPF
3.6.1.3.1.1 Sliding surface definition

The sliding surface is the first step in the design process and it is realized by the following choice of sliding mode-switching functions.

\[
\sigma = \begin{bmatrix}
\sigma_1 \\
\sigma_2 \\
\sigma_3
\end{bmatrix} = \begin{bmatrix}
s_1(x_1 - x_1) + s_2(x_4 - x_4) \\
*s_1(x_2 - x_2) + s_2(x_4 - x_4) \\
*s_1(x_3 - x_3) + s_2(x_4 - x_4)
\end{bmatrix} = \begin{bmatrix}
s_1e_1 + s_2e_4 \\
s_1e_2 + s_2e_4 \\
s_1e_3 + s_2e_4
\end{bmatrix}
\]

(3.31)

where \(e_1, e_2, e_3\) and \(e_4\) are filter current errors for phase A, phase B and phase C respectively. \(e_4\) is the DC capacitor voltage error.

\[
\begin{bmatrix}
\dot{x}_1 \\
\dot{x}_2 \\
\dot{x}_3 \\
\dot{x}_4
\end{bmatrix} = \begin{bmatrix}
I_i \\
I_i \\
I_i \\
V_c
\end{bmatrix}
\]

are reference state vectors. The switching functions given in equation (3.31) are rewritten as,

\[
\sigma = S(X - X) = S(e)
\]

(3.32)

where \(S\) is the sliding mode switching surface. It is defined as \(S = \{X \in \mathbb{R}^n, \sigma(x) = 0\}\) and it represents the trajectory to be tracked by the system state’s variables. The design process is carried forward using the following proposed control law.

\[
U = U_{eq} + U_N
\]

(3.33)
with

\[ U = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}, \quad U_{eq} = \begin{bmatrix} u_{eq}^a \\ u_{eq}^b \\ u_{eq}^c \end{bmatrix} \text{ and } U_N = \begin{bmatrix} u_N^a \\ u_N^b \\ u_N^c \end{bmatrix} \]

In this control law, the equivalent control part \( U_{eq} \) is valid only on the sliding mode surface and the second part \( U_N \) guarantees the existence of the sliding mode. The latter is given by the following.

\[
\begin{align*}
U_N^a &= -\text{sgn}(\sigma_a) \\
\sigma_a &> 0; S_1 = 1; S_4 = 0 \\
&< 0; S_1 = 0; S_4 = 1 \\
U_N^b &= -\text{sgn}(\sigma_b) \\
\sigma_b &> 0; S_3 = 1; S_6 = 0 \\
&< 0; S_3 = 0; S_6 = 1 \\
U_N^c &= -\text{sgn}(\sigma_c) \\
\sigma_c &> 0; S_5 = 1; S_2 = 0 \\
&< 0; S_5 = 0; S_2 = 1
\end{align*}
\]

(3.34)

3.6.1.3.1.2 **Existence of the equivalent control**

The existence of the equivalent control is the necessary condition for the existence of sliding motion over the switching surface \( \sigma(x) = 0 \). In order to keep the state variables on the sliding surface \( S \), the time derivative of \( \sigma \) must be zero along the trajectory and it is given in equation (3.35).

\[
\dot{\sigma} = S \left( \dot{X} - \dot{X}^* \right) = S(AX + BU + C) - S\dot{X} = 0
\]

(3.35)

Substituting \( U = U_{eq} \), the equation (3.35) becomes
\[ U_{eq} = - (SB)^{-1} S \left( AX + C - \dot{X} \right) \]

In equation (3.18), \( \dot{X} = AX + BU + C \) substitute \( U = U_{eq} \) to get,

\[ \dot{X} = AX + BU_{eq} + C \]

\[ \dot{X} = AX + B \left( - (SB)^{-1} S \left( AX + C - \dot{X} \right) \right) + C \]  \hspace{1cm} (3.36)

The equation (3.36) is of the form

\[ \dot{X} = A_{eq} X - B (SB)^{-1} S \left( C - \dot{X} \right) + C \]

where

\[ A_{eq} = A - B (SB)^{-1} SA \]  \hspace{1cm} (3.37)

The following values are chosen for \( R_f = 0.2 \Omega, L_f = 2 \text{mH}, R_{loss} = 0.1 \Omega \) and \( C_{dc} = 2000 \mu \text{F} \) in state equation (3.17) of active filter. The A, B, C and S matrices in the state space equation (3.17) are modeled in per phase basis for finding the \( A_{eq} \). The design values chosen for \( R_f, L_f, R_{loss} \) and \( C_{dc} \) are substituted in the per phase model of the A, B and C matrices given in equation (3.38) to get equation (3.39).

\[ A = \begin{bmatrix} -R_f/L_f & 0 \\ 0 & 1/R_{loss} \ast C_{dc} \end{bmatrix}, B = \begin{bmatrix} V_{dc}/L_f \\ -I_{f,a,b,c}/C_{dc} \end{bmatrix}, C = \begin{bmatrix} -V_s^{a,b,c}/L_f \\ 0 \end{bmatrix} \]

and \( S = (S_1 \ S_2) \)  \hspace{1cm} (3.38)

\[ A = \begin{bmatrix} -100 & 0 \\ 0 & 5000 \end{bmatrix}, B = \begin{bmatrix} 500 \\ -500 \end{bmatrix}, C = \begin{bmatrix} 8558.25 \\ 0 \end{bmatrix} \]
and

\[ S = (1.21 \quad 10.23) \]  \hspace{1cm} (3.39)

The A, B and S matrices given in equation (3.39) are substituted in equation (3.37) to find the \( A_{eq} \). Then the eigen values of \( A_{eq} \) are determined such that the response is non-oscillatory and settles quickly for \( S_1 = 1.21 \) and \( S_2 = 10.23 \).

### 3.6.1.3.1.3 Sliding mode stability

The sufficient condition for the stability in the sliding mode of operation is obtained by having \( \sigma^T \sigma < 0 \), when \( \sigma = 0 \). This represents the sufficient condition for the existence of the sliding surface and ensures the trajectory attraction toward the switching surface. If the initial state is not on the sliding surface S, then the control must be able to force the trajectory to reach the sliding surface and stay on it. Applying the control law given by Equations (3.34) - (3.35), the time-derivative of \( \sigma \) becomes

\[
\dot{\sigma} = S \left( \dot{X} - X \right) = S \left( AX + B \left( U_{eq} + U_N \right) + C \right) - S \dot{X} \tag{3.37}
\]

\[
\dot{\sigma} = SBU_N
\]

\[
\dot{U} = \sigma^T \dot{\sigma} < 0
\]

Substitute, \( U_N = -Sgn(\sigma) \) to get \(-SB Sgn(\sigma) \sigma^T < 0\)

Hence, the time derivative of \( U \) is derived as \( \dot{U} = \sigma^T \dot{\sigma} \)
\[
\begin{align*}
\sigma_1(s_1\frac{X_4}{L_f}\text{sgn}(\sigma_1) + s_2(\frac{X_1}{C_{dc}}\text{sgn}(\sigma_1) + \frac{X_2}{C_{dc}}\text{sgn}(\sigma_2) + \frac{X_3}{C_{dc}}\text{sgn}(\sigma_3)) + \\
\sigma_2(s_1\frac{X_4}{L_f}\text{sgn}(\sigma_2) + s_2(\frac{X_1}{C_{dc}}\text{sgn}(\sigma_1) + \frac{X_2}{C_{dc}}\text{sgn}(\sigma_2) + \frac{X_3}{C_{dc}}\text{sgn}(\sigma_3)) + \\
\sigma_3(s_1\frac{X_4}{L_f}\text{sgn}(\sigma_3) + s_2(\frac{X_1}{C_{dc}}\text{sgn}(\sigma_1) + \frac{X_2}{C_{dc}}\text{sgn}(\sigma_2) + \frac{X_3}{C_{dc}}\text{sgn}(\sigma_3)) < 0
\end{align*}
\]

(3.40)

and to satisfy the above condition $S_2$ should be greater than $S_1$ as $X_4$ is always positive.

The design values given in section 3.6.1.3.1.2 are substituted in Equation (3.40) to verify the sliding mode stability. Thus $S_2 = 10.23 > S_1 = 1.21$ and $V_{dc} = 200$ is always positive. Any practical device for the inverter design has switching frequency limitation. This made to assume in the proposed work, a small hysteresis band of ± 0.5.

### 3.6.1.3.2 Quasi-sliding mode control

The block diagram of QSMC based SAPF is shown in Figure 3.40. In quasi-sliding mode control, the constant switching frequency is achieved by comparing the current error signal with a triangular reference waveform. The switching functions used are same as sliding mode control technique.

The only difference is that triangular reference wave form is used to stabilize the switching frequency by forcing it to be constant and equal to the frequency of the triangular reference signal. Since the current error signal is always kept within the negative and positive peaks of the triangular waveform, the system has an inherent over current protection. The QSMC is also known as constant switching frequency type control. Also the stress on the switching devices and power loss is reduced in QSMC technique.
3.6.2 Simulation Results and Discussion

The performance of the SAPF is evaluated using sliding and quasi-sliding mode control techniques. The parameters used for the simulation are shown in Table 3.9. The simulations are performed using MATLAB under various test conditions to validate the capability of the controllers. The static load and dynamic load compensation using SAPF is examined under SMC and QSMC techniques. However, the simulation results for dynamic load compensation are discussed in section 3.6.2.1. Table 3.10 summarizes the
performance of SAPF with respect to percentage THD of phase-A source current using SMC and QSMC techniques under static load, dynamic load, unbalanced and distorted load condition. It is inferred that SMC based SAPF is found to have satisfactory performance for all the three cases.

### Table 3.9 Simulation system parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase voltage (rms)</td>
<td>70.72 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>2000 μF</td>
</tr>
<tr>
<td>Filter Inductor</td>
<td>2 mH</td>
</tr>
<tr>
<td>Sliding constants $S_1, S_2$</td>
<td>1.23, 10.21</td>
</tr>
<tr>
<td>Desired power factor angle (β)</td>
<td>0 (UPF)</td>
</tr>
</tbody>
</table>

3.6.2.1 Dynamic load compensation

In order to examine the dynamic behavior of the system a 100% step variation of the nonlinear load current is applied at $t = 40$ ms. The three-phase source currents and the THD spectrum of source current for phase-A before compensation are given in Figures 3.41 and 3.42 respectively.

The source currents settle quickly with SMC than QSMC. The compensated three-phase source currents using SMC and QSMC are given in Figures 3.43 and 3.44 respectively. The frequency spectrum of source current for phase-A after compensation using SMC and QSMC are given in Figure 3.45(a) and (b) respectively. Thus, the SAPF has reduced the percentage current THD of source current well below the 5% limit imposed by the IEEE 519 standard using SMC technique but not reduced using QSMC.
technique. The switching pulses to inverter under SMC and QSMC are shown in Figures 3.46 and 3.47 respectively.

It is inferred from Figure 3.46 that the SMC provides dynamic control action at $t = 40$ ms. This helps the percentage THD of source current to reduce from 49.98\% to 0.12\% using SMC. However, the QSMC was able to reduce the percentage THD of source current to 6.95 \% after compensation. This is because, in QSMC when the system reaches the settling time, the frequency of the gate pulses to inverter remains constant irrespective of fluctuation in load current. From the Figures 3.46 and 3.47, it is seen that the switching losses due to SMC is high over QSMC.

Figure 3.41 Source current before compensation for (a) Phase-A (b) Phase-B (c) Phase-C
Figure 3.42 Frequency spectrum of source current for Phase-A before compensation

Figure 3.43 Compensated source current using SMC for (a) Phase-A (b) Phase-B and (c) Phase-C
Figure 3.44 Compensated source current using QSMC for
(a) Phase-A (b) Phase-B and (c) Phase-C

Figure 3.45 Frequency spectrum of compensated source current for
Phase-A (a) Using SMC (b) Using QSMC
Figure 3.46 Switching pulses to inverter under SMC

Figure 3.47 Switching pulses to inverter under QSMC
3.6.2.2 Compensation for distorted and unbalanced load

The SAPF using SMC and QSMC techniques are simulated for distorted and unbalanced load condition. The unbalanced, distorted three-phase source currents and the frequency spectrum of source current for phase-A before compensation are given in Figures 3.48 and 3.49 respectively. The balanced and compensated three-phase source currents using SMC and QSMC are given in Figures 3.50 and 3.51 respectively. The frequency spectrum of compensated source current for phase-A using SMC and QSMC are shown in Figure 3.52(a) and (b) respectively. The percentage current THD of compensated source current for phase-A using SMC is 0.41 % and QSMC is 3.52%. The SAPF has reduced the percentage THD of source current well below the 5% limit imposed by the IEEE 519 standard. Thus, the compensation for unbalanced and distorted load condition by SMC and QSMC is having satisfactory performance.

Figure 3.48 Source current before compensation for (a) Phase-A (b) Phase-B and (c) Phase-C
Figure 3.49 Frequency spectrum of source current for Phase-A before compensation

Figure 3.50 Source current after compensation using SMC for (a) Phase-A (b) Phase-B and (c) Phase-C
Figure 3.51  Source current after compensation using QSMC for (a) Phase-A (b) Phase-B and (c) Phase-C

Table 3.10 Performance comparison of SAPF with respect to percentage THD of source current for Phase-A using SMC and QSMC

<table>
<thead>
<tr>
<th>Cases</th>
<th>Percentage THD of Source Current for Phase-A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without Compensation</td>
</tr>
<tr>
<td>Static load Condition</td>
<td>49.99 %</td>
</tr>
<tr>
<td>Dynamic load Condition</td>
<td>49.98 %</td>
</tr>
<tr>
<td>Unbalanced and</td>
<td>57.79 %</td>
</tr>
<tr>
<td>Distorted Load Condition</td>
<td></td>
</tr>
</tbody>
</table>
It is inferred from the above simulations that when sudden load variation is applied, the sliding mode controller is found to respond quickly and reduce the percentage THD of source current from 49.98% to 0.12%. This is achieved because its switching frequency is varied. When QSMC is applied for the same case the percentage THD of source current reduces to 6.95%. This is because the QSMC has limitations in the switching frequency.
Moreover, the sliding mode controller has better compensation for sudden load current variations because its ON period and OFF period is varied, whereas in quasi sliding mode controller only ON period is varied thereby placing a limitation on the amount of compensation.

The voltage control loop is provided for the capacitor voltage regulation in the sliding strategy of SMC and QSMC, allowing a fast transient response, recovering the steady state in a shorter time, with a low THD in the AC mains current and a unity power factor. Under unbalanced and distorted load condition, performance of both the SMC and QSMC is found to be satisfactory in terms of the percentage reduction in THD of source current from 57.79% to 0.41% using SMC and 3.52% using QSMC.

Thus, the results obtained in the simulation show that SMC based SAPF has better performance in terms of percentage reduction in THD of source current when compared with QSMC under static load condition, dynamic load condition and unbalanced, distorted load condition due to its high switching frequency. However, the QSMC lowers the stress on the switching devices and decreases the power losses.

3.7 SUMMARY

This chapter has focused on the compensation techniques used by D-STATCOM and APLC for mitigating voltage variations and harmonics caused by PE equipment. They are summarized below:

- The five-level diode clamped inverter based D-STATCOM has been modeled using PSCAD/EMTDC software for voltage sag and swell mitigation. The performance of five-level D-STATCOM has been evaluated for a wide range of
operating conditions and is observed to be robust and work satisfactorily for sudden impedance variations of the network by ± 20% resulting in to 75% voltage sag and 80% voltage swell.

• A fuzzy logic based D-STATCOM is proposed to mitigate the voltage sag and swell in low-voltage distribution networks. It is observed that the FD-STATCOM yields smooth control of RMS voltage at the PCC. The FD-STATCOM results are better to those obtained with the conventional PI controller based D-STATCOM for sudden network impedance variations by ± 30 % resulting in to voltage sag and voltage swell. The FD-STATCOM is working satisfactorily for these changes in the loading conditions. But in CD-STATCOM, the \( K_p \) and \( K_i \) settings has to be changed for wide load variations.

• The fuzzy based APLC for the single-phase and three-phase circuit is simulated and the percentage THD measured verifies the reduction of current harmonics. The fuzzy control demonstrates better dynamic behaviour than conventional PI control. The main advantages of this approach are that the inverter system operates simultaneously as an active filter and as power factor compensator.

• A new approach of using wavelet transform for shunt APLC to reduce line current harmonics is proposed. The simulation results verify the reduction in harmonics using this approach.
A comparison between the performance of SAPF with SMC and QSMC techniques under various test conditions is discussed. The simulation results show that SMC based SAPF has better performance when compared with QSMC based SAPF in terms of percentage reduction in source current THD under static load condition, dynamic load condition and compensation for nonlinear load unbalances due to its high switching frequency. However, the QSMC lowers the stress on the switching devices and decreases the power losses.