CHAPTER 6

REVIEW OF PROPOSED POWER QUALITY ENHANCEMENTS

6.1 INTRODUCTION

The increasing use of power electronic devices for different applications such as static power supplies, AC Electric Arc Furnace (AC EAF) and Adjustable Speed Drives (ASD) to improve system efficiency is leading to increasing harmonic distortion levels and poor power factor problems in distribution networks. Consequently, ‘power quality’ has become a serious concern for both utilities and their customers.

The objective of this chapter is to develop techniques for assessment and enhancement of power quality in distribution systems. Two industrial loads viz. UPS in Software park and AC EAF in steel plant are chosen for the present work to understand the feasibility of the developed solution. In the first case, the control concept proposed for the Shunt Active Power Filter (SAPF) realization in SHPF discussed in chapter five is utilized to provide effective solution for the software park. Experimental investigations for without and with SAPF are done to demonstrate the benefits of SAPF to the customers in the software park.

In the second case, the solutions for the current harmonics, voltage harmonics, power factor correction and voltage fluctuation problems due to AC EAF are given through software simulation. SVC is installed for voltage
flicker mitigation and shunt passive filter is designed for harmonic reduction and power factor improvement. The use of SVC allows for efficient voltage flicker mitigation in distribution system. Simulation results for without and with shunt passive power filter are presented.

6.2 HARMONIC MITIGATION USING SHUNT ACTIVE POWER FILTER IN SOFTWARE PARK - CASE I

The schematic diagram of SAPF is shown in Figure 6.1. The control strategy of SAPF is implemented in three stages and the experimental configuration of SAPF is discussed in detail in section 5.3.3 of chapter five. In the first stage, the three-phase source voltages, source currents and DC bus voltage are sensed using hall-effect sensors to get the accurate system information. In the second stage, compensating current signals are extracted from the distorted mains using SRF theory discussed in section 5.3.3.2. In the third stage of control, the gating signals for the solid-state devices of the SAPF are generated using hysteresis-based current control discussed in section 5.3.3.3.

The control block diagram of the SAPF system is shown in Figure 6.2. The SRF theory is utilised for the extraction of the fundamental component of the supply current at PCC. The control also incorporates the command for maintaining the average DC bus voltage of the SAPF. The reference compensation currents for the current-controlled VSI are obtained by subtracting the fundamental components of the supply current computed using SRF theory from the load currents. Finally, the reference and the measured output currents of power converter are compared to generate the switching signals for the VSI through the hysteresis-band current control method.
Figure 6.1 Schematic diagram of shunt active power filter

Figure 6.2 Control block diagram for three-phase shunt active power filter
6.2.1 Details of the UPS system on which the studies are conducted

The single-line diagram of the SAPF installation site at transformer-6 of the Software park, Chennai, Tamil Nadu, India is shown in Figure 6.3.

Field measurements and the waveforms recorded at R phase on the input side of line-interactive type UPS-4 of 400 kVA rating to measure input current THD and input power factor operating at partial load are shown in Table 6.1 and Figure 6.4(a) respectively. The current harmonics of the order 5 and 7 are found predominant compared to other harmonics for the UPS-4 operating on TNEB utility supply (Figure 6.4 (a)). The Crest Factor (CF)
measured is 1.7 and is found to exceed the limits. The input true power factor is found to be low (<0.75).

6.2.2 Experimental Results and Discussions

A full-rated experimental prototype of SAPF for harmonic and reactive power compensation is installed with a 400 kVA UPS at raising main-4 (UPS RM-4) located at the secondary side of transformer-6 in the Software park. The field installation is done to test the harmonic and reactive power compensation performance of the proposed SAPF system. The supply currents, which were highly distorted, and lagging the respective voltage became sinusoidal and in phase with the voltage after the SAPF was put in operation. Thus, the proposed SAPF eliminates the harmonic currents and improve input power factor to be 0.94. The source current THD is measured to be 55.1 % and is reduced to 6.0% after installation of the SAPF. True power factor improved from 0.67 to 0.94. The experimental results for conditions without and with SAPF are presented in Table 6.1 and Figure 6.4 (a-b) to validate the proposed active power filter design. The power rating of the prototype model of SAPF is 60 A\text{RMS}. It is developed by an UPS Manufacturing industry, Chennai, Tamil Nadu, India. The experimental investigations are done to demonstrate the benefits of SAPF to the customers in the software park.

Table 6.1 Comparison of the parameters measured without and with SAPF

<table>
<thead>
<tr>
<th>Different Cases</th>
<th>V</th>
<th>A</th>
<th>kW</th>
<th>kVA</th>
<th>PF</th>
<th>DPF</th>
<th>% Current THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without filter</td>
<td>237.6</td>
<td>110</td>
<td>17.4</td>
<td>25.8</td>
<td>0.67</td>
<td>0.83</td>
<td>55.1</td>
</tr>
<tr>
<td>With SAPF</td>
<td>238.9</td>
<td>82.4</td>
<td>18.2</td>
<td>19.3</td>
<td>0.94</td>
<td>0.96</td>
<td>6.0</td>
</tr>
</tbody>
</table>
6.3 HARMONIC REDUCTION AND VOLTAGE FLICKER MITIGATION IN STEEL PLANT- CASE II

The AC EAF used in the iron and steel plant is an unbalanced, time varying, nonlinear load causing problems to the power system quality. The adverse effects introduced by them are voltage harmonics, current harmonics, low power factor and voltage fluctuations at the PCC. These fluctuations are known as flicker which is regarded as the most difficult power quality problem to be mitigated. These problems bring poor power quality if there is no compensation device and usually causes malfunction of voltage-sensitive facilities nearby. In order to solve the above power quality problems on site and prevent from propagating all over the network, the compensation schemes for harmonics and voltage flicker are designed.
The voltage fluctuation problem is overcome by using voltage stabilisation devices like synchronous condenser with buffer reactor (Miller 1982). The synchronous condenser during installations needs a buffer reactor in series with the furnace bus bar at the upstream of the condenser. As a result, the flicker improvement is achieved only at the PCC and at the expense of an increased flicker at the furnace bus bar. The conventional compensator requires regular maintenance and has limited flicker suppression capability even with buffer reactor. The only type of compensator capable of realizing the benefits of voltage stabilization is active compensator, which has rapid response. The SVC is one of the active compensator proving to be economic and technically advantageous (Acha et al 2001, 2002). Hence, the present work investigates the application of SVC for the mitigation of voltage flicker due to EAF.

The random property of the arc melting process produces harmonic currents, lowering of power factor resulting in additional voltage drop in the power system causing a lower system voltage on the plant buses. The low system voltage increases the melting time and adds to overall plant operating costs (Dugan 1980). Low power factor also results in additional costs in the form of penalties from the electric–utility company. This problem is overcome by using shunt passive power filter (Andrews et al 1996). It is applied to reduce the THD of the AF bus voltage and improve the power factor, which is taken as part of reactive power compensation.

The power quality problems that arise due to EAF is very well studied and analyzed if an accurate model of the EAF is available. Since, the arc furnace operation is highly non-linear and stochastic; it is difficult to develop a precise deterministic model for an arc furnace. Many models are set up based on the static characteristics of AC EAF for the purpose of harmonic analysis (Zheng et al 1998 and Zheng et al 2000). However, based on the
literature survey the exact nonlinear modeling of AC EAF has not been made so far. Hence, in this thesis a nonlinear EAF model based on recorded field data is developed. In this model, the arc furnace is represented by a current source and these currents are the actual measured currents. The compensated supply systems are simulated and the results are discussed using this developed EAF model.

This section discusses a user-defined three-phase EAF load model developed based on field measurement data recorded in 11 kV/250 V distribution system. In this thesis, an attempt has been made to design shunt passive filter bank for harmonic reduction and power factor correction and the application of SVC for the mitigation of voltage flicker due to EAF are presented.

6.3.1 Arc Furnace in Distribution System and Power Quality Analysis

Figure 6.5 is the single-line diagram of four tonne AC EAF and its supply system configuration of a steel works in Chennai, Tamil Nadu, India. The arc furnace is connected to the AF bus through a current-limiting inductance. The AF bus is connected to the HV bus (PCC) through a 2 MVA, 11kV/250V dedicated furnace transformer. The PCC is an 11 kV HV bus.
Field measurements are made at the PCC and in the AF bus to study the magnitudes of current and voltage harmonics due to the nonlinear load without any compensation devices. The current and voltage transformers are used as signal sources at all measurement points. An adequate measurement is accomplished by several days on-site. In addition to harmonic data, power flow and power factor data are also collected to analyse the
system behaviour. The predominant presence of 2, 3, 5, 9 and 15 order harmonics is observed during melting stage (discussed in section 2.4.2 of Chapter two). These harmonic load currents are highly nonlinear and stochastic leading to active and reactive power fluctuation. The changes of reactive power demand with time causes terminal bus voltage fluctuation. The slow and repetitive fluctuations of bus voltage cause flicker, which is rather a nuisance to consumers of electric power.

6.3.1.1 Modeling and Simulation of EAF

A user-defined three-phase EAF load model is built as a current source using recorded field data in 11 kV/250 V distribution system as external input. Thus, it is taken as a real EAF in the simulation system. The simulation results of arc current, arc voltage and arc resistance using field measurement values of EAF during melting cycle are shown in Figures 6.6 and 6.7 respectively. The variation of arc voltage with arc current is shown in Figure 6.8.

![Figure 6.6 Arc voltage and Arc current waveform](image)

Figure 6.6 Arc voltage and Arc current waveform
6.3.2 Compensation scheme design using passive filter and SVC

In order to solve the power quality problems on site and prevent from propagating all over the network, the compensation scheme is designed to solve these power quality problems. First, the shunt passive power filter (SPPF) is used to bypass the harmonics currents and decrease the THD of the AF bus voltage. Then the EAF current and the filter current are summed as the load current. The SVC is then employed for power factor correction of furnace load and as a compensator for the voltage fluctuations caused by the above load current at PCC.
6.3.2.1 Shunt passive power filter design

The harmonic pollution due to EAF is suppressed by installing SPPF to the AF bus. The filter bypass the harmonic currents and the THD level of the AF bus is now well within IEEE 519 harmonic standards. The filter design is carried out by developing a single line model of the utility system supplying the EAF. Load flow and harmonic load flow analysis are performed using ETAP Power Station 4.7.4 package (ETAP 4.7.4 Reference Manual 2003) to calculate the impedance of the supply network for various harmonic frequencies. In order to specify the rating of capacitor and reactor for the filter, the furnace is modeled as a harmonic current generator. This injects harmonic current into the system. The current gets divided in inverse proportion of the impedance offered by these branches to the total impedance offered.

The harmonic filter is then designed to suppress the highest amplitude harmonic currents produced by furnace load. A single tuned harmonic filter is placed at the AF bus. This filter offers low impedance for the harmonic current flow. The supply current measured without and with harmonic filters is not the same. The filter design is performed in an iterative and sequential manner. The load flow results considered for the design of filter and the harmonic load flow details without and with shunt passive filter are given in Table 6.2. The design equations for the single-tuned filter is discussed and given in Appendix 3. The filter design values for the suppression of predominant harmonics during melting stage are tabulated and given in Table 6.3.

The harmonic analysis and filter design involves short circuit and power flow studies of the proposed system. The design of the filter bank
results in an iterative process to optimize the capacitor bank size and filter the unwanted harmonics.

Table 6.2  Power flow and harmonic flow without and with filter during melting stage at Arc Furnace bus

<table>
<thead>
<tr>
<th>Initial load Flow Details</th>
<th>Voltage (kV)</th>
<th>Real Power (kW)</th>
<th>Reactive Power (kVAr)</th>
<th>Load (kVA)</th>
<th>Power Factor</th>
<th>% V THD at AF bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Filter</td>
<td>0.243</td>
<td>1116</td>
<td>813</td>
<td>1380</td>
<td>0.81</td>
<td>22.47</td>
</tr>
<tr>
<td>With Passive Filter tuned at Harmonic Order</td>
<td>Voltage (kV)</td>
<td>Real Power (kW)</td>
<td>Reactive Power (kVAr)</td>
<td>Load (kVA)</td>
<td>Power Factor</td>
<td>% V THD at EAF bus</td>
</tr>
<tr>
<td>5</td>
<td>0.244</td>
<td>1124</td>
<td>691</td>
<td>1319.42</td>
<td>0.85</td>
<td>20.06</td>
</tr>
<tr>
<td>19</td>
<td>0.245</td>
<td>1134</td>
<td>550</td>
<td>1260.34</td>
<td>0.89</td>
<td>6.68</td>
</tr>
<tr>
<td>23</td>
<td>0.246</td>
<td>1146</td>
<td>376</td>
<td>1206.11</td>
<td>0.95</td>
<td>4.78</td>
</tr>
<tr>
<td>8</td>
<td>0.248</td>
<td>1160</td>
<td>162</td>
<td>1171.26</td>
<td>0.99</td>
<td>3.24</td>
</tr>
</tbody>
</table>

Table 6.3  Filter design details for the melting stage

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Power Factor</th>
<th>$X_L(\Omega)$</th>
<th>C (kVAr)</th>
<th>Voltage Rating of C (kv)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Existing</td>
<td>Desired</td>
<td>Achieved</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.81</td>
<td>0.85</td>
<td>0.852</td>
<td>0.019</td>
</tr>
<tr>
<td>19</td>
<td>0.85</td>
<td>0.90</td>
<td>0.899</td>
<td>0.001</td>
</tr>
<tr>
<td>23</td>
<td>0.90</td>
<td>0.95</td>
<td>0.95</td>
<td>0.001</td>
</tr>
<tr>
<td>8</td>
<td>0.95</td>
<td>0.99</td>
<td>0.99</td>
<td>0.004</td>
</tr>
</tbody>
</table>
The arc furnace is modeled as harmonic current source and simulation is carried out using without and with shunt passive filter. From the simulation results, it is found that there is a reduction in the amplitudes of harmonic currents flowing to the source. The comparison of percentage THD for without and with filter during melting and refining stages at AF bus and power factor at AF bus are shown in Table 6.4.

**Table 6.4  Percentage THD and power factor during melting and refining operation at arc furnace bus**

<table>
<thead>
<tr>
<th>AF Bus</th>
<th>Furnace Condition</th>
<th>Melting (Active Arc)</th>
<th>Refining (Stable Arc)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Before Filter</td>
<td>After Filter</td>
</tr>
<tr>
<td></td>
<td>V THD (%)</td>
<td>I THD (%)</td>
<td>V THD (%)</td>
</tr>
<tr>
<td>% THD</td>
<td>22.47</td>
<td>18.76</td>
<td>3.24</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.81</td>
<td>0.99</td>
<td>0.81</td>
</tr>
</tbody>
</table>

It is found that the percentage THD is reduced with filter and it is within the allowable limits of IEEE 519-1992 standards. The allowable limits of harmonics for both voltage and current are given in Appendix 1. The power factor at AF bus is also significantly improved from 0.81 to 0.99.

**6.3.2.2 SVC Design**

The fixed capacitor, thyristor controlled reactor (FC-TCR) is very useful in mitigating voltage fluctuations at PCC. FC-TCR has a fixed
capacitor in parallel with a thyristor-controlled reactor. The compensator is a variable susceptance with no resistive component, as it draws negligible real power from the network. The reactive power is given by equation (6.1) (Acha 2006).

\[ Q_{svc} = -|V_{PCC}|^2 B_{SVC} \]  

(6.1)

where

\[ V_{PCC} = \text{Voltage at PCC} \]
\[ B_{SVC} = (B_C + B_{TCR}) = \text{Equivalent Susceptance of capacitor and inductor.} \]

Equivalent susceptance of the SVC depends on the susceptance of TCR \( B_{TCR} \) and capacitive susceptance \( B_C \). It is given by the Equation (6.2) (Mathur 2002).

\[ B_{TCR} (\alpha) = B_{\text{max}} \left( 1 - \frac{2\alpha}{\pi} - \frac{1}{\pi} \sin 2(\alpha) \right) \]  

(6.2)

where

\[ B_{\text{max}} = \frac{1}{\omega L} \]  

(6.3)

Equations (6.1) to (6.3) suggest that the maximum value of susceptance is obtainable with firing angle alpha at 180 degrees. Since, fundamental reactive current of TCR is directly proportional to the \( B_{TCR} \) it is important that the susceptance is controlled appropriately by a robust control system to supply the required amount of leading reactive power at the PCC.

The SVC has three control system modules viz., measurement system, voltage regulator and a firing pulse generation. Figure 6.9 shows the block diagram of the control system for SVC.
The PCC voltage is passed through a series of low pass and notch filters (at 75 Hz, 50 Hz and 100 Hz) to insure that the measured RMS voltage remains free of any distortion or ripples. The filtered voltage is compared with a reference voltage, which is varied between 0.95 p.u. and 1.05 p.u. (± 5 % of nominal phase voltage). The error signal is used as the input to the voltage regulator, which processes the input error signal and generates a susceptance (reactance) order as an output. The output is proportional to the required reactive power compensation and is a function of firing angle (α). Firing pulse generator processes the input susceptance order and generates the required firing pulses for the thyristors of the TCR.

The digital simulation is performed to study the voltage flicker mitigation without and with SVC connected at the PCC. The following simulation parameters are chosen for SVC control system. $V_{ref} = 1.0$, $G = 5.0$, $T_1 = 0.05$, $T_2 = 0.05$, $Q_C = 50$ and $Q_L = 100$.

Figure 6.9 SVC Control System

Figure 6.10 (a) and (b) shows the RMS voltage at PCC without and with SVC respectively. The simulation results reveal that there is significant decrease in the voltage fluctuation at PCC bus by connecting SVC. Since the SVC compensates the reactive power absorbed by the furnace, the reactive power drawn into AF bus from the distribution system is now very small. Table 6.5 shows the comparison of percentage voltage THD and power factor without and with SVC at PCC. The static compensator not only reduces the voltage fluctuation, but also improves the power factor at PCC. It is also
observed that the percentage voltage THD at PCC is within the limits of IEEE 519 standards.

![Figure 6.10 RMS Voltage at PCC (a) Without SVC (b) With SVC](image)

**Figure 6.10 RMS Voltage at PCC (a) Without SVC (b) With SVC**

**Table 6.5 Comparison of percentage voltage THD and power factor without and with SVC**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without SVC</th>
<th>With SVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>% Voltage THD</td>
<td>4.784</td>
<td>2.21</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.65</td>
<td>0.85</td>
</tr>
</tbody>
</table>
6.4 SUMMARY

This chapter presented the power quality enhancements carried at the Software park and steel manufacturing plant. The investigations are summarized as below:

- The SRF theory based SAPF has been successfully installed and demonstrated at the Software park in TNEB utility for line-interactive type of 400 kVA UPS system to meet IEEE 519 recommended harmonic standards. The experimental results reveal that the SAPF has improved the true power factor by eliminating harmonics and reactive power.

- Field measurements recorded in modern steel plant during melting and refining stages are quite useful in the analysis, providing input data and information to validate system models. The harmonic analysis reveals that voltage fluctuation, percentage THD and percentage individual harmonic distortion for current and voltage are higher than the specified IEEE 519-1992 standards. Hence, SVC is installed at PCC for the voltage flicker mitigation and shunt passive filter is installed at AF bus for harmonic reduction and power factor correction. The simulation results without and with SVC are presented and discussed. The dynamic response and flexible control of SVC allows for efficient voltage flicker mitigation in distribution system. The arc furnace load is modeled as harmonic current source for the design of shunt passive power filter. Simulation results without and with shunt passive power filter are presented.
Analysis of the simulation results reveal that there is a larger reduction in the percentage individual harmonic distortion, percentage THD in voltage and current, higher bus voltage, improved plant power factor from 0.81 to 0.99 at AF bus and elimination of the power factor penalties. Hence, installations of harmonic filters in steel plant are essential and bring real payoffs in the form of improvements in plant productivity.