ABSTRACT

This thesis proposes carrier based Pulse Width Modulation (PWM) schemes to enhance the performance of the three phase three-level NPC inverters and implementation of the proposed PWM schemes in FPGA. The performances of the inverters considered in this thesis are harmonic performance, neutral point voltage variations and low modulation index operation. The harmonic performance of the inverter output can be improved using suitable PWM control technique. Optimal harmonic profile is obtained by centering the middle space vectors in a switching cycle. If the expression of common mode voltage, as calculated for two level inverters, is directly applied to multi-level inverters, the middle vectors may not be centered. So, the harmonic performance is poor. Therefore, to improve the harmonic performance, there is a need to calculate the amount of common mode injection required to center the middle space vectors in a switching cycle. The amount of common mode injection depends on the magnitude of the reference vectors. The common mode voltage is calculated for various cases and is injected into the sinusoidal reference signals to produce modified reference signals. The proposed Variable Common Mode Injection Pulse Width Modulation (VCMIPWM) uses modified reference signals. Due to this, the linear range operation of inverter is increased and harmonic performance is improved. Harmonic performance has been compared for Fixed Common Mode Injection Pulse Width Modulation (FCMIPWM) and VCMIPWM with the existing sinusoidal PWM (SPWM). In order to make use of the theoretical
advantages of the proposed VCMIPWM, this thesis also implements the proposed VCMIPWM using FPGA. Simulation and experimental results are presented.

The major problem in the three-level NPC inverters is neutral point voltage variations. This thesis also analyses the neutral point voltage variations in the three-level NPC inverters and presents how the proposed VCMIPWM reduces them. By equalizing the dwell times of the zero/redundant vectors in a switching cycle, the average of the neutral current due to the small redundant vectors in a switching cycle is made to zero. Proper common mode voltages are calculated for various modulation index regions and are carefully injected with the reference phase voltages. The simulation results show improvement in the neutral point voltage balancing of the inverter with the VCMIPWM scheme compared with the SPWM. Experimental results are shown to verify the practicability of the proposed method.

In low modulation index region, the multi-level inverters have minimum pulse width limitation problems, distortion of the output voltage and current waveforms and several levels of the inverter go unused. This thesis investigates four different PWM techniques and proposes a solution for multi-level inverters which can improve the controllability and output voltage levels in low modulation index region. Comparative analysis has been carried out for different PWM techniques based on MATLAB/SIMULINK simulation results. The proposed THI-Asynchronous dipolar PWM is described along with its
design procedure of FPGA implementation. The results are verified experimentally using a prototype three-level NPC inverter.

As a whole, this thesis proposes simple carrier based PWM scheme called VCMIPWM for three-level NPC inverter to improve the harmonic performance, while maintaining neutral point balance. This work also analyses the problems involved in the MLIs in low modulation index region and proposes THI-Asynchronous dipolar PWM scheme to solve the problems. This thesis adopts recent digital technology of FPGA to implement the proposed PWM schemes. The proposed PWM schemes and FPGA implementation of them improve the performance of industrial drive applications.