CHAPTER 5

REDUCTION OF NEUTRAL POINT VOLTAGE VARIATIONS

5.1 INTRODUCTION

This chapter discusses the causes for the neutral point voltage variations in the NPC inverter and reduction of these by PWM itself.

5.2 CAUSES AND EFFECTS OF NEUTRAL POINT VOLTAGE VARIATIONS

An inherent problem in NPC inverter is neutral point voltage variations. NPC inverter has serious limitation of potential variations in DC-link capacitors which lead to overvoltage stress on the switching devices which in turn results in the failure of the overall inverter system (Won-Sik Oh et al 2006). In Figure 3.1, there are two capacitors $C_1$ and $C_2$. The midpoint between the two capacitors provides neutral point ‘n’. The neutral point voltage is defined as the voltage between the neutral point ‘n’ and the negative DC bus. The neutral point ‘n’ is a floating point where the neutral potential varies, if there is any neutral current $i_n$. The voltage across the DC-link capacitors $C_1$ and $C_2$ must be same. These capacitors are charged and discharged by the neutral current. The neutral point voltage is defined as the voltage between the midpoint of the capacitors and negative DC bus. The neutral point voltage variations may cause failure of the switching devices and also affects harmonic performance of the output voltage of the inverter. This
may cause start-up failure in drive applications. During low speed operation, it may cause more distortion in the output voltage and produces torque ripples.

5.3 REDUCTION METHODS

For the reduction of neutral point voltage variations, already existing methods are discussed in section 1.2.3. The methods are generally classified into open loop techniques and closed loop techniques. Former techniques involve modulation methods and may not need external hardware. Later methods need external hardware. The variations can be reduced by choosing large value of capacitors. By studying the effect of switching vector on neutral point current, the neutral point voltage variations can be reduced by PWM itself without using external hardware.

5.4 EFFECT OF SWITCHING VECTOR ON NEUTRAL CURRENT

The flow of neutral current causes fluctuations of the neutral point potential. The neutral point voltage can be reduced by reducing the magnitude of neutral current and the neutral current is affected by the switching state vectors. For the NPC inverter shown in Figure 3.1, the zero vectors and large vectors do not connect the load terminal to the neutral point ‘n’. The neutral current does not flow through the neutral point. Small redundant vectors either increase or decrease the neutral voltage. The medium vectors affect the neutral point voltage but the direction of voltage deviation is undefined. The effect of the medium vectors is not controllable because it depends only on the duty cycle and the load power factor. To minimize the neutral point voltage variations, the dwell times for small redundant vectors must be equalized in a switching cycle.
The small vectors and medium vectors connect the load terminal to the neutral point ‘n’ according to the switching state vector. The type of phase current, which flows through the neutral point during different states of small voltage vectors and medium vectors, is shown in Table 5.1.

**Table 5.1 Switching state vectors and neutral current**

<table>
<thead>
<tr>
<th>Small redundant voltage vectors</th>
<th>Medium voltage vectors</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vector</strong></td>
<td><strong>Neutral current (iₐ)</strong></td>
</tr>
<tr>
<td>(+00)</td>
<td>iₐ + iₖ = -iₐ</td>
</tr>
<tr>
<td>(++0)</td>
<td>iₖ</td>
</tr>
<tr>
<td>(0+0)</td>
<td>iₐ + iₖ = -iₖ</td>
</tr>
<tr>
<td>(0++0)</td>
<td>iₖ</td>
</tr>
<tr>
<td>(00++)</td>
<td>iₐ + iₖ = -iₖ</td>
</tr>
<tr>
<td>(+0++)</td>
<td>iₖ</td>
</tr>
</tbody>
</table>

5.5 **REDUCTION OF NEUTRAL POINT VOLTAGE VARIATIONS BY VCMIPWM**

For example, consider the half carrier period shown in Figure 4.1. The switching sequence involved in this half carrier period is {(++0) (++-) (+0-) (00-)}. There are four switching state vectors in this sequence. Among these, switching state vectors (++0) and (00-) are small voltage redundant vectors. (++-) is large voltage vector. (+0-) is medium voltage vector. During (++0) switching state, the neutral current iₐ(t) is equal to iₖ(t) as shown in Figure 5.1. During (00-) switching state, iₐ(t) = iₐ(t) + iₖ(t) which is equal to -iₖ(t) as shown in Figure 5.2. When the small voltage redundant vectors (++0) and (00-) are active, the same phase current iₖ(t) causes the neutral current iₐ(t) but in opposite direction. When the large voltage vector (++-) is active, the neutral current is zero as shown in Figure 5.3. When the medium voltage vector (+0-) is active, iₐ(t) is equal to iₖ(t) as shown in Figure 5.4.
Average current within this half carrier period is given by Equation 5.1

\[ I_n = \frac{[t_0 (i_c) + t_1 (0) + t_2 (i_b) + t_3 (-i_c)]}{T_s} \]  \hspace{1cm} (5.1)

Figure 5.1 Neutral current during small redundant vector [++0]

Figure 5.2 Neutral current during small redundant vector [00-]
In SPWM, the dwell times of the redundant vectors $t_0$ and $t_3$ are not same. In VCMIPWM, the switching sequence is not changed. But, the duration of the small redundant vectors $t_0$ and $t_3$ are made equal within the half
carrier period by adding common mode voltage. Hence, the duration of flow of \( i_c(t) \) and \(-i_c(t)\) are equalized and therefore the average value of the neutral current, due to the small voltage redundant vectors, becomes zero. The effect of neutral current is reduced by volt-second balancing.

Equalization of the dwell times of the small redundant vectors maintains the fundamental volt-seconds of the complete cycle. In SPWM, the duration of the small redundant vectors are not same where as in the proposed PWM, common mode injection is made to equalize the duration of these redundant vectors as explained in chapter 4. Due to this equalization, the average of the neutral current becomes zero per half carrier period.

5.6 SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the validity of the proposed carrier based PWM method, simulation for the three-level NPC inverter is carried out using MATLAB-SIMULINK. DC link voltage of the NPC inverter is taken as 120 V. Switching frequency and modulating signal frequency are taken as 1050 Hz and 50 Hz respectively.

The neutral point voltage varies from -20V to +20V for SPWM and it is shown in Figure 5.5. The neutral point voltage varies from -10V to +10V for VCMIPWM and it is shown in the Figure 5.6. The simulation analysis has been done for different modulation indices. The comparison results are given in Table 5.2. From the comparison results, it is observed that the neutral point voltage variations have been reduced by the use of VCMIPWM scheme when compared to SPWM.
Figure 5.5 Neutral point voltage with the SPWM for MI = 0.8

Figure 5.6 Neutral point voltage with the proposed method for MI = 0.8
Table 5.2 Comparison of the range of neutral point voltage variations for the SPWM and VCMIPWM

<table>
<thead>
<tr>
<th>Modulation index</th>
<th>SPWM</th>
<th>VCMIPWM</th>
</tr>
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<tbody>
<tr>
<td>0.1-0.4</td>
<td>-10 to 10 V</td>
<td>-6 to 6 V</td>
</tr>
<tr>
<td>0.5-0.9</td>
<td>-20 to 20 V</td>
<td>-10 to 10 V</td>
</tr>
</tbody>
</table>

The proposed VCMIPWM scheme is implemented in FPGA and tested for three-level NPC inverter with 120V DC supply voltage. 415V AC, 50Hz, 1.05A, 0.37KW, 1380 rpm three phase induction motor is used as load. The NPC inverter is used for v/f control of induction motor. The experimental results are shown from Figure 5.7 to Figure 5.12.

Figure 5.7 shows the switching pulses for NPC inverter. Figure 5.8 shows the output phase voltage and Figure 5.9 shows the output line voltage of the three-level NPC inverter for modulation index of 0.8. Figure 5.10 and Figure 5.11 show the upper capacitor \( (C_1) \) and the lower capacitor \( (C_2) \) voltages of the NPC inverter respectively. The ripple voltage of the upper capacitor is of the order of mV and that of the lower capacitor is of the order of 6V. The capacitor voltages are supposed to be 60V for the DC input of 120V. Due to the neutral voltage variations, the average voltage of the upper capacitor is 62.125V and of the lower capacitor is 49.3472V. Figure 5.12 shows the ac ripple content of the two capacitor voltages as 8V for upper capacitor and 1V for the lower capacitor and their corresponding neutral voltage as 8.32V for the modulation index of 0.8. The experimental results are match with the simulation results. The neutral voltage variations are within ±10V for the DC input of 120V. From the experimental results, it can be seen that the neutral point voltage variations have been suppressed in the VCMIPWM compared to SPWM.
Figure 5.7 Switching pulses for NPC inverter

Figure 5.8 Output phase voltage of NPC inverter for MI =0.8
Figure 5.9 Output line voltage of NPC inverter for MI = 0.8

Figure 5.10 Upper capacitor voltage
Figure 5.11 Lower capacitor voltage

Figure 5.12 Capacitor voltage and neutral voltage ripples
5.7 SUMMARY

In this work, VCMIPWM scheme has been used for three-level NPC inverter for the reduction of neutral point voltage variations. Various common mode voltages are injected into the sinusoidal signals and zero vectors are equalized. The common mode injection does not affect the dwell times of the active vectors in switching cycle. Having equal dwell times for the zero/redundant vectors, the average value of neutral current produced by the small redundant vectors is made zero. By balancing the capacitor voltages, the neutral point voltage variations are reduced. The modified reference signals help to reduce the neutral point potential variations. This reduction ensures better operation of the drive. Without increasing the size of the capacitor bank and without the use of any additional hardware requirements, neutral point voltage variations are reduced using VCMIPWM and this proves the efficiency of the proposed PWM scheme. The effectiveness of the proposed PWM method is verified by simulation results and experimental results.