Chapter 6

Novel Circuits for Pulse Code Modulation
(PCM)-to-Digital Pulse Time Modulation (DPTM)
Conversion and Encryption
6.1 Introduction

Optical Fibre (O.F.) communication systems are becoming popular for long distance communication due to various reasons. Several PTT administrations have installed optical fibre links for various inland and under-sea systems. With advanced single-mode fibres like dispersion shifted and dispersion flattened fibers coming in the market, and with the popularity of the optical fibre amplifiers, intensity modulated direct detection (IMDD) systems are becoming quite popular. A large bandwidth available with these systems is not exploited by existing PCM systems used for data transmission.

An optical fibre is increasingly becoming analogous to free space channel, as a large number of signals are being transmitted simultaneously through the fibre by using various techniques. In view of the paramount importance of message security against eavesdropping, the encryption of signals before transmission through the optical fibre becomes, thus, very attractive.

On the other hand, in certain applications including Broadcasting, Mobile Telephony, Satellite Communication, Global Positioning System (GPS), Remote Sensing etc., a need arises when wireless communication systems are indispensable. Wireless communication allows information to be exchanged between two devices without the use of a physical link. The information is transmitted and received in the form of electromagnetic radiation.
The tremendous growth of portable communication terminals and personal computers has resulted into strong interest in high data transfer rate wireless links for the interconnection of portable devices and for the establishment of Local Area Networks (LANs) [109-111]. Wireless Infrared (IR) communication systems are often used to implement LANs and other interconnections due to various reasons.

Infrared (IR) wireless communication refers to the use of free-space propagation in the region of electromagnetic spectrum between microwaves and visible light. This advantageous property of ultra high frequencies prevents interference between one system and another (due to Line-of-Sight); a short-range communication system in one room cannot be affected by another system in the adjacent room in the same building. IR wireless communication systems have extensive applications for a variety of reasons including low power requirements, high noise immunity, higher security, simple circuitry and low cost compared to conventional Radio Frequency (RF) communication systems.

Pulse Time Modulation (PTM) techniques are preferred to implement both O.F. as well as IR wireless systems due to a number of reasons including high average power efficiency, less circuit complexity, low cost and the possibility of using time division multiplexing. Two popular PTM techniques are Pulse Width Modulation (PWM) and Pulse Position Modulation (PPM). In PPM, the position of the pulse represents the information. This type of modulation technique is preferred in terms of high data transfer rates and best power efficiency, as a single pulse of fixed duration is used to convey the information. However, the clock synchronization between the transmitter and the corresponding receiver is difficult to achieve in PPM transmission. On the other hand, in PWM, the information is carried in the width of the pulses. The width of the pulse
determines the magnitude of the message signal. This type of modulation technique is preferred to PPM due to its easier clock synchronization, though a good data transfer rate is not achieved.

It has been proved that receiver sensitivity below 100 photons per binary digit can be achieved with direct detection using Digital Pulse Position Modulation (DPPM) even at high data rates, thereby exploiting the large bandwidth offered by mono-mode fibres. DPPM systems over mono-mode fibres, thus offer much improved receiver sensitivity. Hence there has been a tendency to use DPPM instead of PCM wherever possible.

Though PPM offers high data transfer rates, it involves complex circuitry for achieving synchronization between the transmitter and the corresponding receiver. On the other hand, PWM, offering low data transfer rates, avoids the need for complex clock synchronization schemes [29]. There are situations when low cost systems (even though offering low data rates) are preferred over fairly complex and costly high bit rate systems. Pulse width modulation circuits are thus fruitful for implementing such cost effective systems with data transfer rates up to 512 Kbits/sec [29].

Since most of the modems for digital communication have been designed for PCM, a PCM-to-DPPM converter is required if DPPM is to be used for data transmission. Similarly, DPPM-to-PCM converter will be needed at the receiver end as most of the destination units operate on PCM signals. Circuits reported in the literature for this purpose are usually complex [112, 131].

In light of the above discussion, novel and simple techniques for Pulse Code Modulation (PCM)-to-Digital Pulse Time Modulation (DPTM) conversion have been presented in this chapter. Section 6.2 presents a PCM-to-DPPM conversion
technique wherein a 3-bit parallel PCM-message signal is directly converted into the corresponding DPPM signal, using the proposed circuit. Receiver circuit for DPPM-to-PCM conversion is also presented. The proposed circuit has been modified to incorporate encryption in the DPPM signal for message security against eavesdropping. The resultant DPPM signal can be demodulated into the original PCM signal and the corresponding circuit for the demodulator has also been presented. The proposed circuits for PCM-to-DPPM conversion are in fact a modification over the corresponding circuits developed and patented by Bhat G. M. and Wasim Ahmad [131]. It can be seen that the circuit complexity has been reduced considerably.

Section 6.3 describes the proposed circuits for PCM-to-DPWM conversion and vice-versa. Experimental results of performance evaluation of the proposed circuits have been presented in this chapter.

6.2 Novel Technique for PCM-to-DPPM Conversion and Encryption

The circuit diagram for proposed PCM-to-DPPM converter is shown in Fig. 6.1. The 3-bit parallel PCM data, to be converted into DPPM signal, is generated by a 3-bit word generator in the given figure. The 3-bit PCM data is applied to the comparator circuit as shown in the Fig. 6.1. Each bit of the PCM signal is individually compared with a corresponding bit of a 3-bit word generated by a 3-bit linear counter. The comparator circuit is implemented using XOR gates and a NOR gate as shown in Fig. 6.2, wherein the PCM bits are applied at I₁, I₂ and I₃ and the linear counter is connected arbitrarily at C₁, C₂ and C₃. The output, Y, of the comparator circuit is given by

\[ Y = (C₁ \oplus I₁) + (C₂ \oplus I₂) + (C₃ \oplus I₃) \]  \ldots (6.1)
The clock signal for the PCM message generator is taken from the most significant bit of the linear counter as shown. Therefore the clock frequency of the linear counter is eight times the message clock. Thus during a particular message available at the output of the PCM generator, the linear counter generates all the eight possible 3-bit words. Each time the linear counter reads '000', the PCM word generator receives a high to low clock and generates a new message word. Now each time a new word is generated from the PCM word generator, it is continuously compared with all the states of the linear counter by the comparator circuit. When the counter generates the same 3-bit word as the PCM word, the comparator output goes to a high state. However, when the counter generates a different 3-bit word, the comparator output will remain low. It is evident that the PCM word will be exactly equal to one out of the eight possible 3-bit words generated by the linear counter in one message interval. Since the PCM word being different from the rest of the seven 3-bit words generated by the counter, the output of the comparator thus remains low during this time. This arrangement divides the message bit interval into eight different non-overlapping sub-intervals and outputs a high pulse on a particular sub-interval during a message word interval. The sub-interval selected and thus the position of the pulse depends upon PCM word. This high pulse is then transmitted as a DPPM signal.

To clarify the working of the proposed circuit, let us consider that the PCM word is '101' and the counter has started from '000'. After the counter receives five clock pulses, the counter reads '101'. When it is compared with the PCM data being already '101', the output of the comparator circuit goes high. For rest of the three states viz. '110', '111' and '000', the comparator output remains in '0' state. Thus a high pulse is transmitted at a particular sub-interval of the message signal. Hence the output signal is a DPPM signal.
The proposed circuit has been modified to form an encrypted system by incorporating a 3-bit pseudo-noise sequence generator circuit as shown in Fig. 6.4. The output data of PN code generator is coupled with the original message taken from the word generator by using modulo-2 addition. The same PN code generator, is used at the receiver circuit to decrypt the encrypted PCM data. The PN-code used at the receiver should be synchronized in phase and frequency with that used at the transmitter.

6.2.1 Receiver Circuits

The circuit diagram for DPPM to PCM converter is shown in Fig. 6.3. The received DPPM signal is applied to one input of an AND gate. The other input of the AND gate is excited by the clock signal, synchronized with the clock signal used at the transmitter. The output of the AND gate generates sampling pulses for the latch circuit. In this circuit 74LS374 has been used for latching purpose. This chip transfers the data to the output on receiving a low to high pulse at its clock input. The inputs of the chip are driven by the 3-bit linear counter. This counter is synchronized with the counter used at the transmitter i.e., the two counters read the same data at any instant of time. When the chip senses a low to high signal at its clock input, the data available at the output of the counter is transferred and latched at the output of the IC 74LS374. Since a low to high pulse is generated at PCM-to-DPPM converter, when the counter output and the PCM signal generator are the same, therefore at the receiver, the same counter state is latched at the output on arrival of the particular DPPM pulse. Hence the DPPM signal is converted back into corresponding 3-bit PCM data.

6.3 Proposed Scheme for PCM-to-DPWM Conversion

Fig. 6.8 shows the circuit diagram of the proposed PCM to DPWM converter. Message words used are generated by a specially designed counter, which
generates all the eight 3-bit words in almost random manner. Each message word is continuously compared with all the possible states of the 3-bit linear counter. When the corresponding bits of a message word and that of the linear counter are the same, the comparator output X becomes low (otherwise it is always held high). Further, the output Y of the OR gate also depends upon the input R received from the most significant bit (MSB) of the modulo-9 counter. This bit also clears all the flip flops of 3-bit linear counter and supplies a clock signal to the message source. Since the clock signal of the message generator is supplied through the MSB of the modulo-9 counter, therefore the clock frequency of the counters is 9 times the message clock frequency (Fig. 6.8). Hence the width of the message word interval will be equal to nine sub-intervals, each sub-interval being equal to the counter state interval. As the 3-bit linear counter goes through only eight different states and occupies only eight subintervals, the ninth sub-interval is thus used as the guard-band between two successive words. This guard-band helps in recovering the PCM data at the receiver faithfully.

To clarify the function of the circuit shown in Fig. 6.8, suppose the message word is ‘100’ and both the counters have started from their clear states. The output will be high till the 3-bit linear counter (CT-1 in Fig. 6.8) reads as ‘100’. As soon as the fourth clock pulse appears at the input of the counter and it counts ‘100’, the corresponding bits of the message word generator and the 3-bit linear counter become the same and therefore the output Y becomes low (the input R of the OR gate being low at this instant). Therefore the width of the output pulse (Y) becomes equal to four sub-intervals (corresponding to message word ‘100’). Further the counter (CT-1) stops counting the rest of the states because no more pulses are supplied, as one of the inputs of the AND gate is held at logic 0 during rest of the states of the counter CT-2. This holds the output Y at logic 0 for the input message period to complete. Now, when the modulo-9 counter assumes
'1000' state, the output Y becomes high and this is where the excursion of next output pulse for the next message word commences. However, the 3-bit linear counter maintains the state '000' till the modulo-9 counter comes in all zero state. At this instant of time the message generator receives a high to low pulse and thus is enabled to pass in the next message word.

6.3.1 Receiver Circuit
The circuit diagram of PWM to PCM converter (Receiver) is shown in Fig. 6.9. The received PWM signal is directly applied to the clock inputs of three D-flip flops. The flip flops receive data from a modulo-9 counter similar to that used at the transmitter and both the counters are synchronized with each other. When the received PWM signal changes from high to low state, the data at the inputs of the D-flip flops gets latched at the output. Since both the modulo-9 counters used at the transmitter as well as at the receiver are synchronized, the instant at which the transitions from high to low take place the data at the output of these counters is same as the data at the output of the message generator at the transmitter. Therefore the latched data at the outputs of the D-flip flops is the original PCM data.

6.4 Experimental Results

6.4.1 PCM-to-DPPM Conversion
The proposed circuits have been implemented in hardware for performance evaluation. The linear counter, word generator and 3-stage PN code generator used in the circuits have been implemented using IC 74LS76, IC 7400 and IC 7486 as shown in Figs. 6.6 & 6.7. The clock signal required by the circuit has been obtained from a function generator. Further, the clock signals used by the transmitter as well as the receiver are assumed synchronous with each other as
the same clock is applied to both the systems for experimental purpose. Both linear as well as random data has been used for the investigation. The word generator as shown in Fig. 6.7 generates all the eight possible 3-bit word combinations in almost random manner. The results of experimental investigation conducted over the proposed scheme are shown in Fig. 6.10. In case of signal encryption for message security, the PN code generator used at the transmitter and at the corresponding receiver have been assumed synchronous. The experimental tests conducted over the encrypted DPPM transmission and reception are found to be satisfactory.

6.4.2 PCM-to-DPWM Conversion

The prototype module of the proposed circuit has been fabricated for experimental investigation. Linear counter as shown in Fig. 6.6(a) has been used to generate all the eight different combinations of a three digit binary word. The modulo-9 counter as shown in Fig. 6.6(c) has been implemented using four JK flip flops with IC7476 and NAND gates with IC7400. This specially designed four stage counter starts from the state ‘0000’ and counts upto state ‘1000’ and then attains again an all zero state. Message words used have been generated by a specially designed counter, which generates all the eight 3-bit words in almost random manner. The waveforms obtained from the circuit are shown in Fig. 6.11. The high frequency clock signal required by the circuit has been obtained from function generator. The recovered PCM data (original message) was found to be correctly received using static test by setting the clock frequency at 1 Hz.
Fig. 6.1: Circuit diagram of the proposed PCM-to-DPPM converter.

Fig. 6.2: Circuit diagram of comparator used in Fig. 6.1.

Fig. 6.3: Circuit layout of DPPM-to-PCM conversion.
Fig. 6.4: Proposed circuit for encrypted PCM to DPPM converter.

Fig. 6.5: Encrypted DPPM-to-PCM converter.
Fig. 6.6(a): Circuit diagram of 3-bit linear counter.

Fig. 6.6(b): Circuit diagram for 3-stage PN-code generator.
Fig. 6.6(c): Circuit diagram of modulo-9 counter.
Fig. 6.7(a): Circuit diagram of 3-bit word generator.

Fig. 6.7(b): State transition diagram of the circuit in Fig. 6.7(a).
Fig. 6.8: Proposed PCM to DPWM converter.

Fig. 6.9: Proposed circuit for DPWM to PCM conversion.
Fig. 6.10(a): Waveforms generated by the proposed circuit shown in Fig. 6.1.
(Upper: Transmitted DPPM signal)
(Lower: Sampling pulses for latch circuit at the receiver)

Fig. 6.10(b): Waveform generated by the circuit shown in Fig. 6.4.
(Upper: Clock Signal)
(Lower: Encrypted DPPM signal)
Fig. 6.11: Waveform generated by proposed PCM-to-DPWM converter.
(Upper: Clock signal)
(Lower: DPWM signal)