CHAPTER-V
5.1 RESULTS AND DISCUSSION

The input–output characteristics of inverter is shown in fig (34). The transition region lies between the input range -0.1 V to +0.68 V. The output falls from -2 V to -0.4 V. The output ranges between -2 V to +1.2 V for the input voltages from -0.1 V to -1.0 V. The threshold input voltage for inverter is about -0.7 volts. The nature of the curve is similar to MOS inverter in conventional system. In conventional system, the input voltage ranges from 0 to -7 V and correspondingly output voltage ranges from -5 V to -0.25 V. The transition exists for the input voltage ranges from 0 to -3 V [112]. For digital signal processing purpose, low voltage ranges are suitable for solving problems. So (+1,-1) representation seems to be more useful.

The input–output characteristics of OR gate is shown in fig (35). The higher level of voltage \( V_{OH} \) exists at +0.50 V and the lower level of voltage \( V_{OL} \) lies at -2.0 V. The input voltage ranges from -0.25 to -0.75 V. When the transition from \( V_{OH} \) to \( V_{OL} \) takes place, the noise margin

\[
\Delta(+1) = V_{OH(max)} - V_{OL(max)} = 0.50 - (-0.25) = 0.75 V
\]

And the noise margin for logic (-1)

\[
\Delta(-1) = -2.0 - (-0.75) = -1.25 V
\]

Initially, the logic level (+1) is at the output voltage \( V_o (+1) = 0.50 \) V. The emitter follower \( \{T_9 \text{ in figure (10)}\} \) cuts off and the emitter follower \( \{T_9 \text{ in figure (10)}\} \) goes to saturation. Hence, the output goes asymptotically towards \( +V_{cc} = 4.86 \) V. Logic level (-1) is reached. When the output voltage becomes -2.0 Volts, the emitter follower \( \{T_{10} \text{ in figure (10)}\} \) cuts off and emitter follower \( \{T_{10} \text{ in figure (10)}\} \) reaches to saturation. Hence, the output reaches to \( -V_{cc} = -4.86 \) V i.e. logic level (-1). The time \( T \) required for transition between logic levels can be written as:
\[ T = RC \log \left| \frac{V_o(1) - (+V_{cc})}{V_o(-1) - (-V_{cc})} \right| \]

\[ T = RC \log \left| \frac{V_o(1) - V_{cc}}{V_o(-1) + V_{cc}} \right| \]

So \[ T = RC \log \left| \frac{0.50 - 4.86}{-2.0 + 4.86} \right| \]

\[ T = RC \log \left| \frac{-4.36}{2.86} \right| \]

\[ = RC \log 1.525 \]

\[ = 0.1829 \text{ RC} \]

The result is compared with OR gate realized by ECL shown in fig. (35). Here, marginal noise \( \Delta 1 = 0.34 \text{V} \) and \( \Delta 0 = 0.33 \text{V} \), \( T = 0.2 \text{ RC} \) [112].

The transfer characteristics of NOR gate is shown in figure (36) and compared with ECL NOR gate. The maximum voltage level \( V_{OH} \) lies at -1.25 V and lowest voltage level \( V_{OL} \) exists at -2.0 V. The input voltage range, for the transition from higher level to lower level is between -0.75 to -0.25.

Noise margin \( \Delta (+1) = 1.25 - (-0.75) = 1.25 + 0.75 = 2.0 \text{V} \)

Noise margin \( \Delta (-1) = -2.0 - (-0.25) = -1.75 \text{V} \)

Time \[ T = RC \log \left| \frac{1.25 - 4.86}{-2.0 + 4.86} \right| \]

\[ T = RC \log \left| \frac{3.61}{2.86} \right| \]

\[ = RC \log 1.262 \]

\[ = 0.1011 \text{ RC} \]

The transfer characteristics of D/A converter are shown in fig. 37(a) and 37(b) for 3 bits and 4 bits respectively. The output voltage ranges for three bits from 7/8 to -7/8 in the steps \( \Delta = 2/8 \). The curve is symmetrical in positive and negative side. There are total 8 levels. The maximum error \( \varepsilon \leq 1/8 \). The accuracy is 3.5 millivolt. The resolution is 14.27%. For two's complement representation, the accuracy is 3.75 millivolt and the resolution is 6.7%. The transfer characteristics of A/D converter is shown in fig. (38). In the table (14)
bipolar binary representation and two's complement representation are shown for comparison. The voltage levels of bipolar binary representation are the same as (+1, -1) binary representation.

Timing circuit using TTL NOT gate in (+1, -1) system has been experimentally tested on CRO. The results have been shown in fig. 17(b,c). We get the same results as obtained from CMOS NOR gate in (0, 1) system. The circuit is slightly modified using two diodes at the output. One of the diodes generates positive clock and other diode negative clock as shown in fig. 17(b,c). Experimentally it is observed that both clocks not have equal amplitudes, positive clock has low amplitude as compared to negative clocks but he time periods are the same. Basic R-S flip-flop can be achieved by NOR gate only in our system. The circuit is similar to R-S flip-flop in (0, 1) system. Here, (-1) represents the reset state and (+1) the set state. The truth table is the same as in (0, 1) system when 0 is replaced by logic (-1). Clocked R-S flip-flop requires NOT gate and NOR gate to provide clock for flip-flop. Here, we employ positive and negative clock as discussed earlier. The circuit of D flip-flop is similar to conventional flip-flop. Here, we use as data either +1 or -1. The hardware realization of J-K flip-flop is similar to conventional system with a little modification. In our system this is achieved by using NOR, NOT and bubbled OR gate.

Fig. 39(a) and 39(b) shows the variation of parcor coefficients or reflection coefficients with the adaptive parameter $\lambda$ of WLPC. The curve actually indicates the different values of coefficients at different cosine of phase angle depending on the ratio of $f/f_s$ where $f_s$ is sampling rate. We get a set of values of $a_{11}$ and $a_{22}$. The reflection coefficients achieved by the author [110] by tapering at the ends of the reflection frequency response. The set of values of reflection co-efficients have been derived from fifteen reflection response samples $R(k)$. The set of values are \{0.3, 0.4, 0.5, 0.4, 0.3\} [Fig.5.18] [110] and the values depend on the ratio $f/f_s$. If we compare the values of parcor-coefficients at different values of $\lambda$, we find that the value of $a_{11} = 0.5$ at
\lambda = 4 \text{ and } a_{11} = 0.4 \text{ at } \lambda = 5, \ a_{22} = 0.3 \text{ at } \lambda = 4, \ a_{22} = 0.5 \text{ at } \lambda = 3 \text{ and } 5 \text{ agree with values of given by author [110] as shown by circle. The parcor-coefficients give the information about the area function of loss less tube representation of vocal tract configuration that would be used in human speech. Fig. (40) indicates the variation of prediction gain in db, with the parameter \lambda for 1st order coefficient. Prediction gain varies between 2db to 5db. The prediction gain for band pass filter for four speakers ranges from 2.5 to 5.2db for 1st order coefficient [34,110] [Fig 5.32] as shown by circle. This shows agreement with experimental results. For low pass filter, the gain ranges from 4db to 8db. In this way, the effect of \lambda gives the best result for wide band speech signal. The gain in (0,1) system in given by equation (8) [106] shown by dotted line in the fig.(40). The nature of the curve is similar but the values are different due to different values of prediction coefficients and co-relation functions in two systems.

Fig. 41(a) and 41(b) shows the variation of correlation function \( r_1 \) with \( \lambda \) for 1st order prediction coefficient and the correlation \( r_2 \) with \( \lambda \) for 11nd order prediction coefficient. The correlation \( r_2 \) varies between 0.9 to -0.75 for \( \lambda = 1 \) to 6. The correlation function of speech signals for different speakers ranges from 0.2 to 0.9 for 11nd order prediction co-efficient [34, 111] [Fig. 5.5] as shown by circle. This is in agreement with the value of \( r_2 \) for \( \lambda = 1 \) to 4 for 11nd order prediction coefficient. For first order prediction coefficient, the correlation value range from 0.7 to 0.95 for different speakers. Our values of correlation function for \( \lambda < 2 \) agree with experimental values as shown by circle. In this way, with the help of \( \lambda \) the correlation function of different speakers can be easily tested. Fig. (42) indicates the variation of power spectral density \( S_{xx}(\omega) \) with digital angular frequency \( \omega \) for LPC. The experimental values due to author [34] are shown by broken line and dashed line due to author [96] [Fig.5]. The nature of our curve is similar to experimental curve but numerical
values are higher than the experimental values. The reason behind this is that the experimental values have been derived at low sampling rate 8 KHz/sample. For accurate digital representation of all speech sounds sampling rate greater than 20 KHz is required. Sampling rate is extremely important in speech signal processing. Speech signals are not inherently band limited. The dotted line shows the power spectral density of WLPC in (0,1) system [106]. The nature of the curve shows similarity with ours. But the values are different due to the fact that the quantization and sampling in the two systems are different.

5.2 CONCLUSIONS

Hardware realizations in this system are well suited for digital signal processing. They are simple and straight and can be easily implemented with a little modification of conventional binary circuit. The positive and negative signals can be processed in a unified way. The modular circuits are possible. High density of VLSI design can be constructed. Although two's complement numbers of conventional binary system is efficient for processing the negative signals. But (+1,-1) binary representation is direct like (0, 1) system contains all the efficiency of two's complement. So for special purposes, the hardware is suitable where a large number of positive and negative signals are needed to be processed in a system. Although various gates require a large number of transistors as compared to conventional system, but the utility of such gates are fruitful whenever handling of positive and negative signals are required for DSP. (+1,-1) binary representation is similar to bipolar binary representation of conventional system in voltage levels but logically, it is an alternative of two's complement representation and more efficient than it in DSP applications.

Sequential circuits and flip-flops in this system for positive and negative signals can be realized in a unified way i.e. on a single chip. A modular circuit is possible and hence; VLSI circuits design of high density is possible. Flip-
flops and registers of this system are useful in DSP applications where positive and negative signals both are processed simultaneously.

Full adder and carry look-ahead adder can be easily implemented in $(+1,-1)$ binary system. The positive and negative carries can be generated by simple XNOR gate. Both types of carries can be propagated using OR gates. Both output carries can be generated by the OR gate and NOR gate. The Carry Look Ahead circuits for negabinary are more complex than our logic system. Extra hardware is needed to convert base $+2$ to base $-2$. The modular form of circuits can be designed and there is no need of sign bit detection. The circuit maintains the symmetry due to inherent symmetry of representation of system $(+1,-1)$. Positive and negative quantities can be directly added in simple way. In digital signal processing where negative numbers are required for arithmetic process, this system is found suitable for VLSI circuit design. The circuit design contains two sum bits and two carry bits. One sum and one carry is selected by control signal. This is the basic difference of conventional adders and adders in this system. Although it requires a large number of hardwares for design but still it is simple and straight and can be easily realized. In digital signal processing especially in DFT and FFT where large number of signed and unsigned numbers are required to be added, the adders of this system are more suitable due to unification of both type of additions on a single chip.

Carry save- add shift (CSAS) and fast –serial parallel (FSP) multiplier can be realized in $(+1, -1)$ binary system. Positive as well as negative numbers can be multiplied in unified way. Analyses of speed shows that time delay of FSP is reduced by approximately $2/3$ in comparison of CSAS which is similar to conventional binary system. The ratio of TFAS/CSAS depends on the number of bits of multiplication. As the number of bits increases, the ratio of two multipliers time also increases and for $n \geq 16$, it becomes almost constant. In conventional binary system, the ratio remains almost constant. If this model
is compared to the 2's complement FSP multiplication, it is found that this model is straight and simple in realization because it requires no sign bit or carry bit extension during partial sum and it also does not require any kind of condition during last sum. The multiplication process always requires similar process at each stage of multiplication. As for as speed is concerned this model requires the same delay time as CSAS multiplier in conventional binary. It is faster than 2's complement FSP multiplier. This is due to the fact that, in 2's complement method extra delay takes place due to XOR gates for conversion of binary to 2's complement number and also during the last sum if MSB of product is 1.

Serial parallel flush multiplier requires n guard bits on data for correct operation. The computational cell has five inputs and two outputs including the gating for partial product formation and clearing sum and carry bits. It requires large number of hardware in comparison of our system for multiplication. Although for 2n-bit product both system require 2n clocks. Thus, the realization of multiplication is straight forward, simple and uniform for positive as well as negative numbers. For VLSI circuit design, this system is useful due to uniform operation for positive and negative data. A single simple cell of multipliers can be constructed for positive and negative data. From speed point of view, this system is superior to the conventional binary system for 2's complement multipliers.

The (+1, -1) binary system can be efficiently applied to processing the speech signals. The unified representation of positive and negative speech signals permit the unified handling of all digits. Digital filters, correlation functions and filter coefficients can be achieved efficiently in simple and straight manner. Due to cellular circuits for multipliers, adders and sub-tractors, higher density in VLSI realization is possible. Linear prediction coding and warped linear predictive coding can be implemented in simpler form. In
general, lattice filter realization of linear or warped linear prediction requires the computation of large number of forward and backward error correlations, which in turn requires large space and time. Here, we require only two, one forward and other backward correlation function for a particular time period. One can compute other correlation functions using the lattice. One can easily obtain the correlation step by step. It requires less space and time. In two's complement representation extra hard-wares for sign detection, overflow detection and for conversion process are required. The cellular circuits for all components of LPC and WLPC are possible. So VLSI design of each component with high density is possible. The study of prediction gain and correlation function with adaptive parameter is helpful in testing the various speech signals from different speakers.