Chapter 7

CONCLUSION AND FUTURE WORKS

7.1 Conclusion

In this thesis, the fabrication of high capacitance density single and bilayer MIM capacitors using anodization process are reported. It is observed that the performance of MIM capacitors is influenced by various fabrication conditions, such as anodization voltage, electrolyte and temperature. These anodic dielectric oxide structures show crystalline, low defect and improved ionic polarization which result higher capacitance density of more than $5\, \text{fF/} \mu \text{m}^2$ and low leakage current density of less than $10\, \text{nA/cm}^2$ with low VCC. These capacitors can be used for future analog and mixed signal applications according to ITRS recommendations for the year 2015.

Single layer MIM capacitors

Fabrication, characterization and performance of anodic alumina MIM capacitors are studied and discussed in Chapter-3. The alumina dielectric layer was anodized for the various anodization voltages using APB solution at low temperature. This yields many MIM capacitors with different dielectric thicknesses. Most capacitors are showing high capacitance density of $> 5\, \text{fF/} \mu \text{m}^2$ and low leakage current density of $< 10\, \text{nA/cm}^2$. The measured VCC and frequency dependence of capacitance are studied using electrode polarization model. The low defect density and strong ionic polarization of anodic alumina
provide a stable frequency dependent capacitance characteristics. Leakage mechanism of anodic alumina is studied using SE and PF emission models. It is observed that large bandgap and barrier height of Al₂O₃ yields low leakage current density. It is predicated that the defect/traps at bulk have deep energy depth of \( \sim 1.5eV \).

The reliability and trap distribution are studied using CVS and RVS experiments respectively. It is observed that the anodic alumina MIM capacitor can operate for more than 10 years continuously for the applied bias of 2V. This is due to strong ionic bonds and low defect density of the anodic Al₂O₃. The low defect density of anodic oxides is due to crystallization during anodic polarization. The trap/defect density was calculated with RVS measurement. It shows that the anodic alumina has very low defect density of \(<10^{16}/cm^3\). Anodic Alumina MIM capacitors show stable and excellent performance, such as low VCC, low leakage current density and high TBD, which are attractive features for analog and mixed signal applications.

Very high capacitance density of \( >30fF/\mu m^2 \) was achieved in barrier type anodic titania MIM capacitors. This high capacitance is achieved due to large dielectric constant of crystalline TiO₂ and a thin interfacial layer of AlTiO alloy. This thin interfacial layer is formed at higher anodization voltage which helps in formation of capacitance and reduction of leakage and VCC of MIM capacitor. However, the leakage current density and breakdown field are poor compared to alumina MIM capacitors. The high defect density during crystallization, poor ionic polarization and large relaxation time exhibit a high sensitivity of capacitance with frequency and temperature.

Various carrier transport mechanisms in dielectrics, such as Schottky emission and Poole-Frenkel emission, are used to study the measured leakage characteristics of anodic titania MIM structure. The asymmetry of leakage characteristics is observed which is due to the present of thin interfacial oxide and non-uniform distribution of trap barrier height at metal-insulator interface. Such defect profile with amorphous region at top interface is the result of nucleation of oxide during anodization. The anodization process and formation of crystalline
phases are explained in detail.

Effect of electrolytes in the performance of TiO$_2$ MIM capacitors is studied in detail. Electrolytes APB and H$_2$SO$_4$ are used for anodization with same anodization voltage. The crystalline states, capacitance density and leakage characteristics are compared for both electrolytes. It was observed that APB offers polycrystalline TiO$_2$ which gives the improved performance than that of H$_2$SO$_4$. High VCC of $>1000$ ppm/$V^2$ and high leakage current density are limiting factors of titania MIM capacitors for the AMS applications. A barrier layer of high bandgap dielectric, such as Al$_2$O$_3$ and SiO$_2$, can be stacked along with TiO$_2$ to reduce the leakage current density and VCC.

**Bi-layer MIM capacitors**

Anodization of Ti/Al metal-couples is introduced in fabrication of MIM capacitors for the first time. This anodized bilayers of TiO$_2$/Al$_2$O$_3$ shows polycrystalline and low defect which are favorable for many AMS and DRAM applications. These capacitor achieved a high capacitance density of $>7fF/\mu m^2$ and low leakage current density of less than $9.1nA/cm^2$ at 3V. It is observed that these capacitors offers low VCC of $<200$ ppm/$V^2$ and quality factor of $>50$. These results are attractive for ITRS recommendation on AMS applications.

The formation of bilayer metal-oxide and crystallization are discussed in detail with outward and inward migration of metal and oxygen ions. It is found that the bottom Al is anodized at higher anodization voltages of $\geq 25V$. The interface traps, Schottky barrier and their temperature dependence are studied using various leakage models. It is observed that the anodic alumina acts like a barrier layer which reduces the leakage current density and VCC. Alumina’s strong ionic bond improves the overall performance of dielectric stack. These all results are suggesting the anodization for future micro and nanoelectronics fabrication. With careful integration of anodization with regular IC fabrication process, one can achieve compact and high performance integrated circuits for various analog, digital and mixed signal applications.
Modeling of CV characteristics

Physics and modeling of CV characteristics of MIM capacitors are useful to analyze the origin of nonlinearities, formation of capacitance, frequency & temperature dependence, and dielectric relaxation in MIM capacitors. Chapter-6 is dedicated for the development of CV models for single and bilayer MIM capacitors. These models show good agreement with experimental results and explores the origin of dependence of capacitance with voltage.

The ionic polarization of metal-oxygen bond and bond distortions are statistically accounted in modeling of CV characteristics of single layer MIM capacitors. The expression hence derived for capacitance exhibits a large dependence with voltage and thickness. This model is used to formulate the expression for nonlinearity coefficient $\alpha(\text{ppm}/V^2)$. It is predicted that the bond distortion due to applied field is the origin of nonlinearities in many dielectrics. It also predicts that non-polar dielectrics show low VCC compared to polar dielectric materials. The formula is also used to predict the required thickness of dielectric material to meet the ITRS requirement. It predicts that the thickness of dielectric layer should be $>100nm$ for $\varepsilon_r > 30$ to achieve a low voltage linearity coefficient of $<100\text{ppm}/V^2$. These observation are highly useful to inquire the effectiveness of fabrication/oxidation process to meet the ITRS requirements.

Modeling of CV characteristics of bilayer MIM capacitors accounts the ionic, orientation and Maxwell-Wagner polarization mechanisms. The accumulation of charges at the interface of high to low conductance materials due to applied field increases the effective dielectric constant of stack. Maxwell’s time varying accumulation process at pure insulator interface is considered to calculate the charge density of dielectric interface. This charge density is used to calculate the interfacial capacitance, named as $C_{MW}$. The proposed model for CV characteristics shows a good agreement with measured results by introducing carrier tunneling probability of dielectric stack. It is observed that the MW polarization is dominant at low frequencies ($<10kHz$). This model indicates that the nonlinearity can be suppressed by choosing the similar permittivity dielectric materials for fabrication of multilayer MIM
7.2 Scopes for future work

Anodization

High-k oxide thickness in ULSI circuits is scaled down to meet the industry requirements. However, the reliability of oxides and quality of oxidation are challenging problems in fabrication process. It is observed that the application specific values like EOT and leakage current density are limiting factors of oxide thickness. Other than these challenges, the high-k dielectrics in nanoelectronics should hold good thermal and chemical stability with good interfacial properties. In this thesis, the experimental results show that the anodic oxides have large potential to solve all these issues. It is observed that the anodic oxides have low structural defects, improved ionic polarization and good thermal stability compared to many other oxidation schemes. Therefore, one can introduce the anodization of high-k dielectrics for fabrication of MOS capacitors and MOSFET structures to achieve high performance. The low defect and improved ionic polarization will largely support on dielectric reliability of oxides.

Annealing is a common process to reduce the structural defects and oxygen vacancies in the dielectrics. However, it may reduce the quality of metal electrodes or substrate. Anodic oxidation can be used to reoxidize the dielectric layer prepared by other techniques, such as ALD, PVD and CVD. The breakages and structural defects in dielectrics can be removed at low temperature itself. However, the metal or substrate should be chemically independent of anodization which needs suitable electrolyte. Anodization is one the nonlithography techniques which utilizes the masking cum chemical etching process for micrometer level fabrications. This practice largely reduces the time and cost of IC fabrication.

The bilayer or multilayer anodization have lots of potential in organic and semiconductor transistor fabrication. The accumulated charges at interface of two materials form a channel in organic transistors. This accumulation process is inherent in anodic bilayer structure at low
frequencies. Therefore, the anodization of a bilayer of dielectric material stacks can be used to fabricate organic transistors. This process can replace conventional fabrication process with low cost. However, the metal stack of different metals has to be anodized by single electrolyte which limits the choice of metals. This needs a detailed study on anodization of various metal couples and their interfacial properties.

**On modeling**

Kinetic Monte Carlo simulations of leakage current for single layer was reported by few others. The stress induced leakage current or tunneling probabilities for the uniform defect profiles are utilized in those works. However, the defect distribution will be high at interfaces and uniform at bulk. Moreover, the field distribution at defects or dipoles are not uniform. Monte Carlo simulation of leakage characteristics with nonuniform defect profiles and nonlinear field distributions can be proposed. This simulation is highly useful for modeling of ultra thin oxide layers for nanoscale devices and circuits. Also the study of defect profile and dipole mechanisms of fabricated layer can be extracted using simple empirical relation. This empirical equation is useful for semiconductor device and circuit simulations.

Monte Carlo simulation of leakage current in dielectric stack is not yet reported as of our knowledge. Unlike the single layer case, the nonuniform field distribution at each layer and interface should be treated with quantum mechanical components. The study of leakage mechanisms of multilayer dielectric stack using Monte Carlo simulation is challenging in association with traps and dipoles. In Chapter-6, the modeling of nonlinearity is calculated using the ionic polarization, orientation polarization and interfacial polarization. This model can be extended to multilayer dielectrics. The field distribution in each layer and the dielectric properties should be incorporated to model the capacitance-voltage characteristics. This model is very useful in many cases. For instance, the cancellation of positive VCC of high-$k$ layer with negative VCC of SiO$_2$ is proved experimentally by many
authors. It is observed that increment of the SiO$_2$ thickness reduces the $\alpha$-VCC lesser than 100 ppm/$V^2$. However, the capacitance will decrease intern. Therefore, the multilayer model for $\alpha$-VCC can calculate the optimum thickness to get highest possible capacitance density for the minimum VCC as per the ITRS recommendation for AMS applications.