Chapter 5

ANODIC BILAYER MIM CAPACITORS

5.1 Introduction and Motivation

Bandgap of dielectric material is inversely proportional to the dielectric constant [Robertson, 2004, Mise et al., 2010]. Nobuyuki Mise et al have shown that effective barrier thickness of high-k MIM structures decrease with increment in permittivity [Mise et al., 2010]. Reduction in barrier height and effective thickness of dielectric layer shall further lead to high leakage and poor reliability. High-k dielectric stack engineering has emerged in fabrication of MIM capacitor to solve these issues. Usually a thin barrier layer of large bandgap dielectric material (Al$_2$O$_3$, SiO$_2$) is stacked with very high dielectric constant material (ZrO$_2$, TiO$_2$ and HfO$_2$). Recently, many authors have reported on various bilayer stack MIM capacitors such as HfO$_2$/SiO$_2$, HfTiO/Y$_2$O$_3$, TiO$_2$/SiO$_2$ and SrTa$_2$O$_7$/SrTiO$_3$ [Kaynak et al., Kim et al., 2004, Wu et al., Tsui and Cheng, 2010].

Fabrication of multilayer stack of dielectric materials using anodization is not common. Few possible approaches can be adopted: 1) Anodization of individual layer after deposition of each metal layer 2) Simultaneous anodization of thin film layers of metals. The former one is easier but time consuming and may not yield the expected stack. When the second metal layer is deposited on anodized first layer, the metal ion may migrate which degrades the formation of stack. In case-2, the electrolyte should anodize all metals simultaneously.
Figure 5.1: Schematic model of anodization of superimposed layer [Yao et al., 2010].

Since, the top metal layer is oxidized first, it will block the migration of oxygen to second metal layer. However, on both the cases, rarely reports are available.

Anodic oxidation of superimposed multilayer metals was studied in detail by J. Perriere et al about three decades ago [Perriere et al., 1978, Perriere and Siejka, 1983a,b]. In those works, Ta-Nb, Al-Ta, and Al-Nb couples were anodized and observed that the bottom metal-oxides are amorphous. Later, G. E. Thompson et al have reported the anodization Al-Zr bilayer using 0.1M ammonium pentaborate solution at 25°C [Shimizu et al., 1997]. Recently, Yao Lei et al have reported the fabrication procedure for TiO_2/Al_2O_3 dielectric stack using combined sol-gel and anodization processes [Yao et al., 2010]. Sol-gel coated TiO_2 on aluminum foil has been anodized using aqueous ammonium adipate solution in 25°C. It is observed that at higher annealing temperatures (600°C) the crystalline transformation from amorphous to anatase in TiO_2 was observed [Yao et al., 2010]. The schematic model of anodization of superimposed layer is shown Fig. 5.1 [Yao et al., 2010]. But sufficient works are not available for MIM capacitor with bilayer TiO_2/Al_2O_3 using anodization process.

This chapter presents the fabrication and characterization of a bilayer TiO_2/Al_2O_3 MIM capacitor using anodization process. Our bilayer capacitors show a high capacitance density, low leakage current density and low VCC which are close to ITRS recommendations for
the year 2015. The formation of bilayer, crystalline properties and conduction mechanisms are studied in detail. It is observed that the crystalline oxides and excellent polarization properties in dielectric stacks have improved the performance of MIM capacitors.

5.2 Fabrication process flow

A 100nm SiO$_2$ was grown on Si (100) substrate and thoroughly cleaned by deionized water. Over that, a bilayer of 15nm Ti on 100nm Al is deposited using electron beam evaporator with tungsten filament at a pressure of $8 \times 10^{-5}$ mBar. This Ti/Al film was anodized potentiostatically using non-aqueous solution of ammonium pentaborate dissolved in ethylene glycol (20g/l) by the same size of platinum cathode. Oxidation was done for various anodization voltages of 15V, 20V, 25V and 30V till the anodization current density reduces to 1µA/cm$^2$. Only three-quarters of sample area was dipped in the electrolyte to avoid etching for bottom electrode. This forms a barrier type anodic TiO$_2$ and bilayer of TiO$_2$/Al$_2$O$_3$ at low and high anodization voltages respectively. After cleaning thoroughly by deionized water, a 50nm thick Al top electrode was deposited on the samples using thermal evaporation with the shadow mask area of $\sim 0.61 mm^2$. Samples AT1 and AT2 are single layer TiO$_2$ MIM capacitors and samples AT3 and AT4 are bilayer TiO$_2$/Al$_2$O$_3$ MIM capacitors.

Figure 5.2: SEM cross section image of anodized region before top electrode deposition, (a) AV = 15V (b) AV = 20V (c) AV = 25V and (d) AV = 30V.
Figure 5.3: SIMS depth profile of all samples (a) AV=15V (b) 20V (c) 25V (d) 30V

5.3   Physical and Electrical properties

5.3.1   Formation of bilayer and crystallization

SEM cross-section of anodized regions of all the samples are shown in Fig. 5. 2. The titanium film is anodized fully at low anodization voltages ($\leq 20V$) with a thin ($< 2\text{nm}$) interfacial layer of AlTiO. The bottom Al was also anodized at higher anodization voltages and formed $\text{Al}_2\text{O}_3$. Anodization voltage was restricted to 30V due to delamination of TiO$_2$ from bottom Al$_2$O$_3$ at higher anodization voltage (AV $> 30V$, not shown).

Fig. 5. 3 shows the depth profile of all the four samples using secondary ion mass spectrometry (SIMS) in positive mode with 1kVCs. It shows the ion distribution of Ti, Al, O, Si, Ti-O and Al-O. Al bottom electrode is also slightly anodized at low anodization voltages (15V and 20V). It is observed that the intensity of Al-O is significant near TiO$_2$/Al interface (Fig 2(a) and 2(b)). This is due to the outward migration of Al ion which forms a thin interface layer of AlTiO. Notably, the composite layer reduces the effective thickness
of TiO$_2$ which shall help in formation of capacitance and reduction of leakage. The AlTiO layer reduces the inward migration of oxygen ions into Al bottom electrode. However, at higher anodization voltages (25V and 30V), the inward migration of oxygen ion increases which forms a thin layer of Al$_2$O$_3$. It is observed that outward migration of Al into TiO$_2$ is increased which increases the thickness of AlTiO composite layer.

X-ray diffraction patterns of the anodized samples for various anodization voltages are shown in Fig. 5.4. It is observed that the crystalline phases of TiO$_2$ anatase and rutile are present at low anodization voltages (<20V). At higher anodization voltages, the crystalline Al$_2$O$_3$ ($\gamma$–Al$_2$O$_3$) emerges at $2\theta = 65.5^o$. Crystallization of anodic TiO$_2$ has been addressed by many authors. But nucleation/crystallization of anodic bilayer oxides was studied by very few authors [Shimizu et al., 1997, Yao et al., 2010].

Crystallization and formation of bilayer are addressed based on the observations of Piyus Kar, H. Habazaki et al, K. Shimizu et al and Yao Lei et al [Shimizu et al., 1997, Yao et al., 2010, Kar, 2010, Habazaki et al., 2003]. Step-by-step process flow is shown in Fig. 5.5. During the anodization, the amorphous TiO$_2$ has been formed at initial stage. This oxide is capable of conducting electrons and oxygen evolution at solution-oxide interface. The applied anodization voltage/field impacts at the metal/insulator interface with high energy. This leads to transformation of amorphous to rutile TiO$_2$ with bulk defects [Kar, 2010].
the same time, the outward migration of boron ions stabilizes the amorphous TiO$_2$ at outer oxide-surface [Habazaki et al., 2003]. Anatase phase transition occurs at defect sites (above rutile region). The low activation energy at defects helps this heterogeneous nucleation of anatase TiO$_2$ [Kar, 2010]. During these processes, anodization of Al results a thin amorphous AlTiO which reduce further evolution of oxygen. At higher anodization voltages, both the migration of oxygen and evolution of electrons into Al region increase and forms a thin layer of crystalline Al$_2$O$_3$ near TiO$_2$/Al$_2$O$_3$ interface. For voltages greater than 30V, the density of defect sites at TiO$_2$/Al$_2$O$_3$ interface increases rapidly and forms local cavities. This ruptures the oxide due to pressure within defects and delaminate TiO$_2$ from surface of Al$_2$O$_3$.

5.3.2 Capacitance and Voltage linearity

The capacitance and leakage current density were measured using semiconductor parameter analyzer (HP4155C). Figure 5. 6 (a) shows the C-V characteristics of all four samples at room temperature. AT1 and AT2 are showing high capacitance density (> 30fF/µm$^2$) compared to other two samples which shows that the top Ti alone was anodized with a very thin interfacial layer of AlTiO. Thin interfacial layer acts like a tunnel barrier and helps in formation of capacitance [Woo et al., 2012]. Formation of bilayer TiO$_2$/Al$_2$O$_3$ at higher anodization voltages reduces the capacitance density. However, the capacitance density of AT3 is 10.32fF/µm$^2$. 
Figure 5.6: (a) C-V characteristics of anodic TiO$_2$/Al$_2$O$_3$ MIM capacitor at a temperature of 25°C (b) Frequency dependence of capacitance and Quality factor

Voltage coefficients of capacitance (VCC) are extracted from C-V characteristics using $C(V) = C_0(\alpha V^2 + \beta V + 1)$, where $C_0$ is the capacitance at voltage of zero, $\alpha$ and $\beta$ are the quadratic and linear coefficient of capacitance. The extracted $\alpha$ (ppm/V$^2$) reduces from 995 to 150 ppm/V$^2$ as anodization voltage increases from 15V to 30V. This is due to low defect alumina which plays a dominant role in formation of capacitance. Fig. 5. 6 (b) shows the measured capacitance density with frequency of all the samples for applied bias of 3V at room temperature. In TiO$_2$ MIM capacitors, capacitance decreases as frequency increases due to the poor ionic polarization. AT3 and AT4 are exhibiting a high capacitance density of $> 20$ fF/µm$^2$ at low frequency upto 5KHz due to space charge polarization at TiO$_2$/Al$_2$O$_3$ interface. The capacitance density does not vary much after 10KHz due to the strong ionic polarization of $\gamma$-Al$_2$O$_3$. The inset of Fig. 5. 6 (b) shows the calculated quality factor for all samples where the bilayer samples show quality factor of $>50$ for upto 800KHz.

5.3.3 Leakage characteristics and Temperature dependence

The leakage characteristics of bilayer MIM structure was measured by injection of electrons from top and bottom electrodes. Fig. 5. 7 shows the measured leakage current density as a function of applied voltage for all the samples at room temperature. It is observed that most of the samples are showing high degree of asymmetry at forward and reverse biases and leakage current of AT3 and AT4 drastically reduces. These are due to formation of AlTiO
Figure 5.7: Measured leakage current density for all samples at room temperature

![Figure 5.7](image)

Figure 5.8: Measured leakage current density at various temperatures (a) AT2 sample (b) AT4 sample

interfacial layer and TiO$_2$/Al$_2$O$_3$ stack.

Conduction mechanism of MIM structure is analyzed using Schottky emission (SE), Poole-Frankel emission (PFE) and trap assisted tunneling (TAT). Fig. 5. 8 (a) and 5. 8 (b) show the measured current density of the samples AT2 and AT4, respectively, as a function of applied voltage at various temperatures. At low field ($-1V < V_{bias} < 1V$), the current density is less than $10nA/cm^2$ and no significant variation is observed due to change in temperature. This shows that the emission of electron is blocked by large effective barrier height which is independent of temperature. Unlike AT2, each J-V characteristic in sample AT4 exhibits a sharp transition or kink at low fields ($1V < V_{bias} < 2.5V$). It is also observed
Figure 5.9: Extracted barrier height at various temperatures. (a) AT2 in forward bias, (b) AT2 in reverse bias (c) AT4 in forward bias (d) AT4 in reverse bias that the kink is occurring at lower bias voltages for higher temperature. This shows the presence of positive traps at the interface of TiO$_2$/Al$_2$O$_3$. At high fields (|V$_{bias}$| $\geq$ 2.5V), the leakage increases rapidly and varies with temperature.

The leakage due to SE mechanism is expressed as [Chakraborty et al., 2005],

$$J_{SE} = A_R T^2 \exp \left\{ -\frac{1}{kT} \left( q\phi_B - \beta_{SE} \sqrt{E} \right) \right\}$$  \hspace{1cm} (5.3.1)

where $\beta_{SE} = (q^2/4\pi\varepsilon_0\varepsilon_r)^{1/2}$ and $A_R$ is Richardson’s constant (= $1200cm^{-2}k^{-2}$), $\varepsilon_0$ is permittivity of the free space and $\varepsilon_r$ is dielectric constant of the insulator (considered as 40), $\phi_B$, T and E are Schottky barrier height, temperature and applied electric field respectively.

Fig. 5.9 (a) and 5.9 (b) show the extracted Schottky barrier height for AT2 at forward and reverse bias respectively. A small difference of 0.05eV in bottom and top metal/TiO$_2$ interface is observed at low fields. This is due to AlTiO layer at the bottom electrode interface. It is also observed that the change in barrier height for various temperature is
more significant in forward bias than the reverse bias. This indicates the interface layer and crystalline layer near bottom metal/insulator interface are highly sensitive with temperature. Similarly Fig. 5.9 (c) and 5.9 (d) show the extracted Schottky barrier height for AT4 at both biases. In forward and reverse biases, a difference of \( \sim 0.25 \text{eV} \) is observed in AT4 compared to that of AT2. This is due to outward migration of Al into TiO\(_2\) region. Variation in extracted barrier height at forward bias is less significant with temperature compared to reverse bias. This is due to presence of barrier type anodic Al\(_2\)O\(_3\) which shows stable barrier height and traps which are insensitive to temperature.

The kink at low fields due to positive traps at the interface of TiO\(_2\)/Al\(_2\)O\(_3\) is explored using TAT mechanism. Houssa et al used TAT model which has not included the insulator/insulator interface trap [Houssa et al., 2000]. In our present study, a term \( \phi_{ii} \) has...
been introduced to specify the trap barrier height of insulator/insulator interface traps. The modified TAT model can be expressed as,

\[ J_{TAT} = A_T N_t \exp \left( \frac{(qV_{stack} - \phi_1 + \phi_2 + \phi_t - \phi_{ii})}{k_BT} \right) \] (5.3.2)

Here \( \phi_1 \) and \( \phi_2 \) are barrier height at Al/TiO\(_2\) and Al\(_2\)O\(_3\)/TiO\(_2\) interface respectively. \( \phi_t \) is trap barrier height at TiO\(_2\) region. The new term \( \phi_{ii} \) specifies the positive traps at insulator/insulator interface with negative sign. If \( \phi_1 \) and \( \phi_2 \) are known, the \( \phi_t \) and \( \phi_{ii} \) can be extracted using Eq. 5. 3. 2 from leakage characteristics of AT4 (Fig. 5. 8 (b)). The barrier heights used are \( \phi_1 = 3.29eV \) and \( \phi_2 = 2.29eV \) [Hickmott, 2005]. Trap barrier height \( \phi_t - \phi_{ii} \) were extracted for \( 1V < |V_{bias}| < 3V \), and shown in Fig. 5. 10(a) and 5. 10(b) for forward and reverse bias respectively. Since \( \phi_{ii} \) has no effect in forward bias (Fig. 5. 10 (a)), it is considered as zero. This results the barrier height of traps (\( \phi_t \)) available at anodic TiO\(_2\) region. In reverse bias, the extracted trap barrier height shows a large difference at kink points. From the difference of trap barrier heights in forward and reverse bias, the relative trap barrier height \( \phi_{ii} \) values are plotted as a function of voltage and show in Fig. 5. 10(c). The values of \( \phi_{ii} \) for various temperature at kink points are shown in Fig. 5. 10 (d). It is clear that relative barrier depth of traps at Al\(_2\)O\(_3\)/TiO\(_2\) interface decreases with temperature.

5. 11 (a) gives a comparative study of our results with others in terms of capacitance density and VCC. It is observed that the samples AT3 and AT4 show high capacitance density and low VCC comparable with other bilayer MIM capacitors [ITRS, 2011, Kaynak et al., 2011, Kim et al., 2004, Wu et al., 2012, Tsui and Cheng, 2010]. The structures with SiO\(_2\), such as HfO\(_2\)/SiO\(_2\) and TiO\(_2\)/SiO\(_2\) show a very low VCC (less than 100\( ppm/V \)) due to the canceling effect. Fig. 5. 11 (b) compares the leakage characteristics of various stacked MIM capacitors with ITRS recommendations. Samples AT3 and AT4 are meeting the requirements of ITRS and show the least values among the recent works in bilayer MIM capacitors [ITRS, 2011, Kaynak et al., 2011, Kim et al., 2004, Wu et al., 2012, Tsui and Cheng, 2010].
5.4 Summary

In this chapter, fabrication and characterization of barrier type TiO$_2$/Al$_2$O$_3$ MIM capacitors using anodic oxidation technique are presented in detail. These capacitors show more than 7fF/$\mu$m$^2$ and a low leakage current density of 6.56nA/cm$^2$ at 3V at room temperature. The formation and crystallization of TiO$_2$/Al$_2$O$_3$ stack are discussed with XRD and SIMS facility. Frequency dependent of capacitance and quality factor are measured from 1KHz to 1MHz. A high capacitance density of more than 10fF/$\mu$m$^2$ is observed at low frequencies which is due to space charge polarization. Using SE and TAT models, the effective barrier heights of metal/dielectric and dielectric/dielectric interface traps are extracted for various temperatures. It is found that they are sensitive to temperature asymmetrically with bias due to outward migration of Al ions. The unique properties of anodization, such as low defect, improved polarization and crystallization, exhibit high performance MIM capacitors for RF and Mixed signal ICs. At lowest fabrication cost, the anodization process can be an attractive fabrication method for multilayer dielectric stack for wide ranges of nano-scale applications.