Chapter 2

LITERATURE AND TECHNOLOGY REVIEW

2.1 Evolution of MIM capacitors

Jack Kilby’s first integrated circuit was an RC phase shift oscillator which was constructed with one transistor, three resistors and one capacitor as shown in Fig. 2.1 [Kilby, 1959]. The first IC capacitor was a planar $pn$-junction capacitor, made of diffusing n-type layer in p-type substrate with single top electrode plate [Kilby, 1959]. Later, MOS like capacitors were also proposed with a stack of SiO$_2$/Si between two metal plates [Kilby, 1959]. However, it was claimed that the capacitors showed a better stable capacitance than $pn$-junction capacitance. This shows that the inversion layer at SiO$_2$/Si was not formed which is similar to “Metal-Insulator-Metal” capacitor.

Figure 2.1: First Proposed Integrated Circuit - RC Oscillator
From 1960 to 1990, many researchers developed various planar capacitors for wireless radio circuits. MOS capacitor fabrication methods were optimized and became most successful technology. High-\(k\) materials, such as Si\(_3\)N\(_4\), Al\(_2\)O\(_3\), TiO\(_2\) and Ta\(_2\)O\(_5\), were predominately used in capacitors as insulators to increase the capacitance density. In 90s, the nanostructured thin film technologies were evolved in fabrication of single chip RFICs [Surganov, 1994].

MOS capacitor was the only candidate for analog and mixed signal IC technologies. However, it showed undesirable variations in capacitance with voltage and poor interface quality with high-\(k\) materials. These variations are tolerable in some applications, such as DRAM and few analog applications. However, it can not be acceptable in high precision circuits, like digital signal processors (DSP), analog-to-digital (AD) and digital-to-analog (DA) cases [T. Iida and Akiba, 1990, Onge et al., 1992]. The precision is not about the value of capacitance, but it is a measure of sensitivity of capacitance with voltage and temperature. The precision is measured using voltage coefficient of capacitance. VCC highly depends on the interface property of metal/insulator or polysilicon/insulator, thickness of dielectric layer and quality of dielectric material. Those three properties are largely affected by the fabrication method.

Polysilicon-insulator-polysilicon (PIP) capacitors replaced MOS capacitors in 1999 [T. Iida and Akiba, 1990, Onge et al., 1992, Chen and Hou, 1999]. PIP capacitors were
realized using LPCVD grown polysilicon layers and with high temperature deposition of dielectric, such as thermal oxidation [T. Iida and Akiba, 1990, Onge et al., 1992]. However, PIP capacitors also suffered variation of capacitance with voltage due to the depletion effect at polysilicon/substrate interface and associated parasitic capacitance. With careful reduction of depletion effect, PIP capacitors had shown lower voltage linearity than MOS capacitors [Onge et al., 1992]. However, the in-situ doping of polysilicon and additional mask for etching had increased the manufacturing cost compared to CMOS technology. Though PIP capacitor technology was well established, poor RF compatibility at very high frequencies, poor quality factor (<50) due to resistive losses at polysilicon plates, intra-element parasitic capacitance and lossy silicon substrate were the dominant weaknesses [Onge et al., 1992, Ng et al., 2005].

Metal electrodes were used to replace the polysilicon top and bottom contacts, particularly Pt or TiN [Ng et al., 2005], so they were called as “Metal-Insulator-Metal (MIM) capacitors”. It was constructed over top of metal lines to avoid series resistance and cross talk between silicon substrate. PIP and MIM capacitors are shown in Fig. 2.2 (a) and 2.2 (b) respectively. Fig. 2.2 (a) shows the cross-section view of PIP capacitor which had been placed over a field oxide. The voltage linearity of this capacitor is shown as inset of Fig. 2.2 (a). It can be observed that increase in doping of polysilicon improved the VCC. This is due to reduction of depletion at polysilicon/insulator interfaces. On the other hand, MIM capacitors with Al$_2$O$_3$ and AlTiO$_x$ dielectric layer are shown in Fig. 2.2 (b) which exhibit a very low dependence with voltage and frequency. This is due to improved metal/insulator interface and field distribution of MIM capacitors lies within two metal electrodes.

MIM capacitors are usually fabricated as follows. First of all, the wafer or substrate will be cleaned using RCA cleaning technique. An insulating layer of SiO$_2$ of higher thickness is deposited using thermal oxidation. A bottom electrode of metal or metal-alloy thin film will be deposited using PVD or thermal evaporation. Nanostructured dielectric thin film will be
Table 2.1: Analog and Mixed-signal MIM Capacitor Technology Requirements: Near future deposited by unique deposition tools. High temperature annealing with O\textsuperscript{2} will be applied to crystallize and reduce the oxygen vacancies in bulk dielectrics. After cleaning thoroughly using deionized water, top metal electrode will be deposited as similar to bottom electrode. Lithography and etching process will be carried out to ground or excite the bottom electrode. The selection of electrode metal, metal deposition technology, dielectric material, dielectric deposition technology, and thickness of each layer are considered based on the applications.

### 2.2 Technology Roadmap for MIM capacitors

#### 2.2.1 ITRS for Analog, RF and Mixed signal ICs

International Technology Roadmap for Semiconductor (ITRS) is a non-profit organization which predicts the future scopes on the advancement of ICs fabrication. It draws a map of future requirements in IC manufacturing and modeling. For Analog and Mixed signal processing [ITRS, 2011], it specifies the technology requirement for MIM capacitor, in terms of various performance parameters. Table 2.1 and Table 2.2 show the near and far future requirements of MIM capacitor according to ITRS 2011 [ITRS, 2011]. It is expected to achieve more than 10\(fF/\mu m^2\) for the year 2018 with low leakage of 10\(nA/cm^2\) and low VCC of less than 100\(ppm/V^2\).

#### 2.2.2 Road map for DRAM

Dynamic random access memories (DRAM) is also one of the most popular applications of MIM capacitors. The MIM capacitors should have a low leakage current density of less than
### Table 2.2: Analog and Mixed-signal MIM Capacitor Technology Requirements: Far future

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2017</th>
<th>2018</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance density ($fF/\mu m^2$)</td>
<td>7</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Voltage linearity (ppm/V$^2$)</td>
<td>$&lt;100$</td>
<td>$&lt;100$</td>
<td>$&lt;100$</td>
<td>$&lt;100$</td>
<td>$&lt;100$</td>
</tr>
<tr>
<td>Leakage (A/cm$^2$)</td>
<td>$&lt;10^{-8}$</td>
<td>$&lt;10^{-8}$</td>
<td>$&lt;10^{-8}$</td>
<td>$&lt;10^{-8}$</td>
<td>$&lt;10^{-8}$</td>
</tr>
<tr>
<td>$\sigma$ Matching (%·µm)</td>
<td>0.3</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Q factor</td>
<td>$&gt;50$</td>
<td>$&gt;50$</td>
<td>$&gt;50$</td>
<td>$&gt;50$</td>
<td>$&gt;50$</td>
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</table>

100nA/cm$^2$ and a very high capacitance density of 25fF/cell for DRAM applications [Mise et al., 2010]. High-k materials and suitable top/bottom electrodes shall provide best solution in this regard. Fig. 2.3 shows a typical DRAM cell with Ta$_2$O$_5$ MIM capacitor. Here top and bottom electrodes are made up of TiN with W interconnect. MIM capacitors in DRAM has significant difference from that of AMS applications. Due to the location of DRAM cell, i.e., below the first metal line (bit line), the high temperature dielectric material preparation could be acceptable.

![Figure 2.3: DRAM cell with Ta$_2$O$_5$ MIM capacitor](image)

In DRAM IC, number of bits per chip, miniaturization (about 40% per year) and reliability improvement are key challenges in recent years. In recent ITRS charts, the demand of low leakage current density ($10nA/cm^2$) and very high capacitance density ($>25fF/\mu m^2$) were identified for industrial requirement which are independent of the equivalent oxide thickness (EOT) of the capacitor. Fig. 2.4 shows the roadmap of MOS and MIM technologies in DRAM, developed by M. S. Yoo. MIM capacitors with high-k
dielectrics were utilized for DRAM applications during the last decade. The future demand is ultra high density capacitors with improved dielectric reliability and reduced process variations. This indicates that the lithography and masking techniques need to be replaced with advanced methods.

2.3 Fabrication technologies

Conventional SiO$_2$ ($k = 3.9$) and Si$_3$N$_4$ ($k = 7$) dielectric MIM capacitors have shown capacitance density of $\leq 2 fF/\mu m^2$ with low VCC of $> 100 ppm/V^2$ and very low leakage current density of $< 1 nA/cm^2$ [Onge et al., 1992]. These capacitors occupy a large area to get a high capacitance since they possess low capacitance density. At the same time, for DRAM requirement - this area increases about 5 times. This leads to increase in noise, IC size and high fabrication cost. On the other hand, ITRS restricts the maximum temperature of dielectric processing up to 400°C to make compatibility with back-end fabrication processes [ITRS, 2011].

In this regard, many high-$k$ materials were introduced as dielectrics in MIM capacitors in the last decade. Along with high capacitance density, many studies were dedicated to achieve low voltage linearity, low leakage current density and improved reliability. This
section covers a detailed review on various high-

$k$ materials and their processing techniques for MIM capacitors. It spotlights the processing methodologies and addresses the challenges in MIM capacitor with the available roadmaps. In this review, the MIM dielectric layer is classified into single layer and stack of high-$k$ dielectrics. These dielectrics materials can be binary, ternary and few ferroelectric oxide materials.

2.3.1 Earlier and Recent trends

DRAM and AMS ICs need simple, low fabrication temperature and low cost dielectric deposition method. Various fabrication methods have been proposed in MIM capacitor technology to meet such requirements, such as atomic layer deposition (ALD), sol-gel, sputtering, thermal oxidation, anodic oxidation and physical/chemical vapor deposition (PVD/CVD). Using these technologies, various dielectric structures, such as single layer, bilayer and multilayer, were developed for MIM capacitors for the past ten years. Most popular oxides - such as $\text{Al}_2\text{O}_3$, $\text{TiO}_2$, $\text{Ta}_2\text{O}_3$ and $\text{HfO}_2$ are extensively investigated. However, some of the rare earth and ferroelectric dielectric materials are also receiving attention for high density MIM capacitors.

Single-layer MIM capacitors

$\text{Al}_2\text{O}_3$ is an attractive high-$k$ dielectric material with energy band gap of 8.3eV, dielectric constant of 9 to 10, and heat of formation of 399K.cal/mol [Lee et al., 2000]. The intrinsic dielectric properties of $\text{Al}_2\text{O}_3$, i. e. dielectric-relaxation and reliability, were extensively investigated in [Allers et al., 2003, Lee et al., 2000]. It was concluded that $\text{Al}_2\text{O}_3$ is a reliable dielectrics for MIM capacitors which shows high reliability and low leakage current density [Allers et al., 2003]. Chen et al reported $\text{Al}_2\text{O}_3$ MIM capacitor using thermal oxidation and subsequent annealing at $400^\circ\text{C}$ [Chen et al., 2002]. This 12nm thick $\text{Al}_2\text{O}_3$ MIM capacitor with TaN as bottom electrode shows a capacitance density of $5\ f\text{F}/\mu\text{m}^2$ and leakage current density of $10\text{nA/cm}^2$ [Chen et al., 2002]. The capacitor shows a high VCC of $>2000\text{ppm}/V^2$ with less sensitivity of capacitance with frequency. In the same work, it
was reported that doping Ti with Al₂O₃ results in AlTiOₓ (an alloy of Al₂O₃ and TiO₂). AlTiOₓ MIM capacitor showed a high capacitance density of 10fF/µm² [Chen et al., 2002]. However, it shows a strong dependence of capacitance with temperature and frequency. This is due to weak Ti-Al-O bond, defect sites at bulk and metal/insulator interface and poor oxidation due to doping of Ti ions. Yu et al reported fabrication of Ta/Al₂O₃/Ta MIM capacitor with 13nm of dielectric layer using ALD. This capacitor shows a capacitance density of 2.2fF/µm² and leakage of 4.9 × 10⁻⁸A/cm² [Yu et al., 2003a]. Later, Ding et al have also fabricated Al₂O₃ MIM capacitor of same thickness with TaN electrodes. It shows a high capacitance density of 6.05fF/µm², low leakage current density of 48nA/cm² with high breakdown field of 8.61MV/cm [Ding et al., 2007]. This capacitor shows acceptable VCC of less than 795ppm/V² [Ding et al., 2007]. It was observed in Yu et al work that the bottom Ta electrode was also oxidized and formed a thin interfacial layer which reduces the capacitance density. This indicates that TaN electrodes have good thermal stability and improved interface quality with high-k oxides. It was identified that the conduction mechanism is dominated by TAT and FP hopping mechanisms in both capacitors.

15nm ALD Al₂O₃ MIM capacitor with TiN as electrode was reported by S. Bécu et al [Be’cu et al., 2006]. The capacitor showed a capacitance density of 4.5fF/µm². In this work, the modeling of capacitance variation with temperature was reported. It was observed that the capacitance increased linearly with temperature which is due to increase in permanent dipole moment at higher temperatures. It is also observed that VCC has quadratic relation with applied electric field due to displacement of metal cation from equilibrium [Be’cu et al., 2006]. Preparation of nanostructured Al₂O₃ thin film using anodic oxidation for MIM capacitors has been carried out by few authors in recent years [Hourdakis and Nasiopoulou, 2010, 2012]. Hourdakis et al reported the performance of MIM capacitors with anodic Al₂O₃, using anodization electrolytes as sulfuric acid and citric acid aqueous solutions [Hourdakis and Nasiopoulou, 2010, 2012]. The sulfuric acid
and citric acid form barrier type and porous type anodic alumina films respectively. It is observed that barrier type alumina shows a high capacitance density of $7fF/\mu m^2$ with low VCC of less than $500 ppm/V^2$. Barrier type anodic oxides have a large ionic polarization and low defect density [Hickmott, 2007, Kosjuk and Odynets, 1997].

HfO$_2$ is one of the attractive materials for dielectrics in nanoscale devices which has been extensively studied by many researchers during the last decade. With dielectric constant of $\sim25$ and bandgap of 5.7eV, HfO$_2$ replaced SiO$_2$ and reduced short channel effects in MOSFET. Mise et al reported that HfO$_2$ is promising and optimum dielectric material for DRAM technologies [Mise et al., 2010]. Using PVD technology, 50nm HfO$_2$ MIM capacitor achieved a capacitance density of $3.3fF/\mu m^2$ with a leakage current of $90nA/cm^2$ at 5V [Perng et al., 2004]. A high density MIM capacitor with HfO$_2$ was fabricated by Yu et al [Yu et al., 2003]. It shows a capacitance density of $13fF/\mu m^2$ for the 10nm thick film using ALD [Yu et al., 2003]. Hu et al demonstrated the fabrication of 56nm thick HfO$_2$ MIM capacitor using pulsed-laser deposition (PLD) [Hu et al., 2002]. This capacitor shows a high capacitance density of $>18fF/\mu m^2$ and leakage current density of less than $2nA/cm^2$ for 3V. No annealing or sintering was performed during fabrication since the deposition was carried out at temperature of 200$^o$C [Hu et al., 2002]. The VCC reduces from 134 to $44 ppm/V^2$ as frequency increases due to the reduction in polarization of dipole.

Tantula or Ta$_2$O$_5$ is one of the stable dielectric materials like Al$_2$O$_3$ whose dielectric constant varies from 25 to 30. Tu et al and Jeong et al demonstrated the Ta$_2$O$_5$ MIM capacitors using MOCVD [Tu et al., 2003, Jeo, 2004]. These capacitors showed a capacitance density of less than $5fF/\mu m^2$ with very low VCC of $9.9 ppm/V^2$, this is due to higher thickness of Ta$_2$O$_5$ [Tu et al., 2003, Jeo, 2004]. However, the leakage current density was predicted as 100 times greater than that of Al$_2$O$_3$ and SiO$_2$ [Tu et al., 2003, Jeo, 2004]. Sedghi et al reported Ta$_2$O$_5$ MIM capacitor using wet anodization. The reliability and temperature dependent leakage characteristics are reported in this investigation. It was observed that the trap barrier height of Ta$_2$O$_5$ is 1.3$V$ which is close to that of Al$_2$O$_3$.  

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<table>
<thead>
<tr>
<th>Ternary oxide</th>
<th>Capacitance (fF/µm²)</th>
<th>Leakage current density (A/cm²)</th>
<th>VCC (ppm/V²)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfAlOx</td>
<td>3.5 to 6</td>
<td>10⁻⁴ at 3V</td>
<td>143 to 583</td>
<td>[Hota et al., 2009]</td>
</tr>
<tr>
<td>(HfO)(Al₂O₃)</td>
<td>3.5</td>
<td>10⁻⁶ at 1V</td>
<td>180</td>
<td>[Yu et al., 2003b]</td>
</tr>
<tr>
<td>HfLaO</td>
<td>7.5 to 16</td>
<td>10⁻⁸ at 1V</td>
<td>&gt;1000</td>
<td>[Zhang et al., 2010]</td>
</tr>
<tr>
<td>HfTbO</td>
<td>13.3</td>
<td>10⁻⁴ at 3V</td>
<td>2667</td>
<td>[Kim et al., 2003]</td>
</tr>
<tr>
<td>TaZrO</td>
<td>12</td>
<td>10⁻⁶ at 1V</td>
<td>&gt;1000</td>
<td>[Inoue et al., 2006]</td>
</tr>
<tr>
<td>SrTaO</td>
<td>10</td>
<td>10⁻⁸ at 3V</td>
<td>200</td>
<td>[Goux et al., 2006]</td>
</tr>
<tr>
<td>BiTaO</td>
<td>10</td>
<td>10⁻⁸ at 3V</td>
<td>600</td>
<td>[Goux et al., 2006]</td>
</tr>
<tr>
<td>AlTaOx</td>
<td>17</td>
<td>10⁻⁷ at -2V</td>
<td>-</td>
<td>[Yang et al., 2003]</td>
</tr>
<tr>
<td>SrTiO3</td>
<td>44</td>
<td>10⁻⁷ at 1V</td>
<td>&gt;3000</td>
<td>[Peng et al., 1993]</td>
</tr>
<tr>
<td>TiTaO</td>
<td>14.3</td>
<td>10⁻⁷ at 2V</td>
<td>634</td>
<td>[Chiang et al., 2005]</td>
</tr>
<tr>
<td>TiCeO</td>
<td>10.3</td>
<td>10⁻⁷ at 2V</td>
<td>866</td>
<td>[Cheng et al., 2008]</td>
</tr>
<tr>
<td>TiZrO</td>
<td>5.5</td>
<td>10⁻⁸ at 32V</td>
<td>105</td>
<td>[Cheng et al., 2008]</td>
</tr>
<tr>
<td>TiLaAlO</td>
<td>24</td>
<td>10⁻⁷ at -2V</td>
<td>&gt;1000</td>
<td>[Cheng et al., 2010]</td>
</tr>
<tr>
<td>TiLaYO</td>
<td>16.4</td>
<td>10⁻⁷ at -2V</td>
<td>&gt;1000</td>
<td>[Cheng et al., 2010]</td>
</tr>
<tr>
<td>PrTixOy</td>
<td>10</td>
<td>10⁻⁴ at 2V</td>
<td>&gt;1000</td>
<td>[Wenger et al., 2005]</td>
</tr>
</tbody>
</table>

Table 2.3: A performance comparison of MIM capacitor with ternary oxides

Titanium oxide or Titania (TiO₂) is an attractive material that has evolved with considerable interest in variety of applications such as gas sensors, photovoltaic devices and capacitors [Wisitsoraat et al., 2009, Gratzel, 2001, Chiang et al., 2005]. TiO₂ naturally exists in 3 crystalline phases namely rutile, anatase and brookite, with dielectric constant of 40 to 100 and energy band gap of ∼3.0 eV [Mantzila and Prodromidis, 2005]. However, its dielectric constant can be improved by various treatments, particularly annealing till 800°C [Lin et al., 1999]. Recently, TiO₂ MIM capacitors have been fabricated using thermal oxidation [Chiang et al., 2005] and DC magnetron sputtering [Stamate et al., 2009]. Thermal oxidation and DC magnetron sputtering yield MIM capacitor with high leakage current density (> 10⁻⁴ A/cm²) and capacitance variation ΔC/C₀ of more than 10⁴ ppm [Chiang et al., 2005, Stamate et al., 2009]. Also the poor polarization and high defect density in bulk and metal-insulator interface are leading to high dependency of capacitance with frequency [Stamate et al., 2009]. This is due to the structural defects/traps available in bulk oxide and near to metal/insulator interface. The high leakage current density of Ta₂O₅ and TiO₂ MIM capacitors are due to their low bandgap of 4.2eV and 3eV respectively.
Few rare earth dielectrics were also employed in MIM capacitors in the last decade. J. Yang et al and M. Yang et al have reported MIM capacitors with $\text{Sm}_2\text{O}_3$ and $\text{La}_2\text{O}_3$ respectively. These capacitors were fabricated with optimization on PVD which show a high capacity of more than $7.5\,\text{fF/\mu m}^2$ [jun Yang et al., 2009, Yang et al., 2004]. It was observed that the VCC reduces from $1000\,\text{ppm/V}^2$ to $100\,\text{ppm/V}^2$ when the dielectric thickness was increased [jun Yang et al., 2009, Yang et al., 2004]. $\text{Y}_2\text{O}_3$ and $\text{Pr}_2\text{O}_3$ were also used in MIM capacitors which yield more than $8\,\text{fF/\mu m}^2$ with VCC of $14100\,\text{ppm/V}^2$ and $1310\,\text{ppm/V}^2$ respectively [Durand et al., 2006, Wenger et al., 2004]. $\text{Lu}_2\text{O}_3$ MIM capacitors with Ni top electrode shows a capacitance density of $7.5\,\text{fF/\mu m}^2$ and leakage current density of $50\,\text{nA/cm}^2$ at 1V [Mondal and Pan, 2011]. It shows a good reliability of 0.51% of $\Delta C/C_0$ at 3V for the continues stress of 10 years.

It has become a trend that by superimposing or doping one dielectric material on another, called ternary dielectric. Ternary oxides have the ability to alter the bandgap and dielectric constant by optimizing the doping. Table 2. 3 classifies the achievement of ternary oxides based on Hf, Ta and Ti. It is observed that all ternary oxide MIM capacitors show high capacitance density of $> 5\,\text{fF/\mu m}^2$. However, most of them are suffered by high leakage current density and VCC. This is due to poor oxidation of superimposed metals which results in structural defects and poor polarization issues.

**Dielectric stack MIM capacitors**

Mise et al have shown that effective barrier height of high-$k$ MIM structure decreases with increment in permittivity [Mise et al., 2010]. Fig. 2. 5 shows the comparison of conduction band diagram for various high-$k$ MIM capacitors based on equivalent oxide thickness (EOT) [Mise et al., 2010]. If the direct tunneling of charges from metal to metal alone being considered, the effective barrier thickness drastically reduces for the increase in dielectric constant. This shall further lead to high leakage and poor reliability of oxide. High-$k$ dielectric stack engineering has emerged in fabrication of MIM capacitor to solve these issues. Usually, a thin barrier layer of large bandgap dielectric material ($\text{Al}_2\text{O}_3$, $\text{SiO}_2$) is
stacked with very high dielectric constant material (ZrO$_2$, TiO$_2$ and HfO$_2$). Recently, many authors have reported on various bilayer stack MIM capacitors such as HfO$_2$/SiO$_2$, HfTiO/Y$_2$O$_3$, TiO$_2$/SiO$_2$ and SrTa$_2$O$_7$/SrTiO$_3$ [Kaynak et al., Kim et al., 2004, Wu et al., Tsui and Cheng, 2010]. Two motivations are often visible in various reports of dielectric stack MIM capacitors for Analog/Mixed signal application:

1. Reduction of VCC by canceling positive VCC of an oxide using negative VCC of SiO$_2$.

2. Reduction of leakage current density by introducing large bandgap materials.

Negative voltage coefficient of capacitance of SiO$_2$ has been investigated by many researchers for the last two decades, however it has been modeled accurately by Phung et al [Phung et al., 2011]. The orientation polarization of permanent dipoles is significantly reduced with applied electric field compared to ionic or electronic polarizations [Phung et al., 2011]. This leads to reduction in capacitance or negative VCC. This behavior is helpful in canceling positive VCC of many high-k dielectric materials. Kim et al proposed
such possible stack and achieved very low VCC of $14\text{ppm}/V^2$ [Kim et al., 2004]. Stack of 12nm ALD HfO$_2$ and 4nm of PVD SiO$_2$ with TaN electrodes shows a capacitance density of $6fF/\mu m^2$ with low leakage of $10nA/cm^2$ at 4V [Kim et al., 2004]. Using similar canceling idea, Yang et al [Yang et al., 2009] have reported fabrication of MIM capacitors with rare earth Sm$_2$O$_3$ stacked on SiO$_2$ which showed low VCC of less than $100\text{ppm}/V^2$ with capacitance density of $7fF/\mu m^2$. However it shows high leakage compared to HfO$_2$/SiO$_2$, as $10^3nA/cm^2$ at 4V. This is due to low bandgap of Sm$_2$O$_3$ and dominant PF emission at low voltages [Yang et al., 2009]. TiO$_2$/SiO$_2$ stack MIM capacitor has been demonstrated recently by Wu et al [Wu et al., 2012]. The capacitor exhibits a high capacitance density up to $11.2fF/\mu m^2$ and very low VCC of $30\text{ppm}/V^2$. Here 14nm TiO$_2$ film was deposited using e-beam evaporation at room temperature, followed by furnace annealing in O$_2$ ambient at 380°C. The resulting TiO$_2$ is amorphous with dielectric constant of 31. Later, polycrystalline TiO$_2$ with dielectric constant of 111 is achieved by rapid thermal annealing in the presence of N$_2$ at 500°C [Wu et al., 2012]. Pr$_2$Ti$_2$O$_7$ on SiO$_2$ stacked MIM capacitor was reported by Wenger et al, which results $3.2fF/\mu m^2$ with VCC of less than $100\text{ppm}/V^2$. Due to low dielectric constant of SiO$_2$ the total capacitance of MIM capacitor was decreased in these works.

Laminated HfO$_2$/Al$_2$O$_3$ stack MIM capacitors were reported by Ding et al for RF applications [Ding et al., 2004]. The capacitors exhibit a capacitance density of more than $4fF/\mu m^2$ with acceptable VCC of $200\text{ppm}/V^2$ at 1MHz. It was found that the thickness of Al$_2$O$_3$ significantly reduces the VCC and sensitivity of capacitance with frequency. Along with HfO$_2$, many high-$k$ oxides, such as HfO$_x$C$_y$N$_z$ [J.-M. Park and Kang, 2007], LaAlO$_3$ [L. Zhang and Cho, 2010], were stacked and proposed in recent years. MIM capacitor with laminated Ta$_2$O$_5$/HfO$_2$/Ta$_2$O$_5$ stack was developed by Jeong et al [Jeo, 2004]. The capacitor shows a capacitance density of $4fF/\mu m^2$ and low VCC of $16.9\text{ppm}/V^2$ with high leakage of $10^{-7}A/cm^2$ at 3.3V [Jeo, 2004]. 3nm Al$_2$O$_3$ on 40nm Ta$_2$O$_5$ as dielectric stack, MIM capacitor was reported by Ishikawa et al which showed a capacitance density of
4.4\(fF/\mu m^2\) and VCC of 400\(ppm/V^2\) [Ishikawa et al., 2002]. However, the capacitance density increased to 9.2\(fF/\mu m^2\) with VCC of 3580\(ppm/V^2\) while the Ta\(_2\)O\(_5\) thickness was reduced to 16nm [Ishikawa et al., 2002]. Here Al\(_2\)O\(_3\) acts like a barrier layer which reduces the leakage current density. The Al\(_2\)O\(_3\)/Ta\(_2\)O\(_5\) show a low leakage current density of 10\(^{-8}\)A/cm\(^2\) compared to HfO\(_2\)/Ta\(_2\)O\(_5\). This is due to large bandgap of Al\(_2\)O\(_3\) compared to HfO\(_2\).

It is observed that most of the dielectrics of MIM capacitors were not crystalline. This is one of the reasons for low dielectric constant and high VCC since the ionic polarization of dipole are suppressed in amorphous dielectrics. Al\(_2\)O\(_3\) and Sm\(_2\)O\(_3\) show high performance amongst all single layer dielectrics. On the other hand, double layer dielectric stacks were meeting ITRS recommendations in terms of leakage current density and VCC. This is due to presence of barrier layer whose ionic or orientation polarization suppress the dependence of dielectric constant with applied field. This further improves the quality factor and dielectric reliability. However, multilayer MIM capacitors are suffering with low capacitance density. In general, the polarization, defect profile and thickness of dielectrics are influencing the performance of MIM capacitors, irrespective of single of multilayer dielectrics. This indicate that an alternate high quality oxidation with low fabrication temperature is required for preparation of MIM capacitors.

### 2.3.2 Anodization for Nano-capacitors

Anodic oxidation or Anodization is an electrochemical process which results low defect metal oxides. It can be performed using an anodizing cell which consists of a container with an electrolyte solution, anode, cathode and DC/AC power supply. Since the nature of electrolyte, temperature and voltage are highly influencing the anodization process, the necessary measurement set-up can be added further. A typical anodization cell is shown in Fig. 2. 6. Anode is the metal to be oxidized and cathode can be a non-reacting metal or alloy. Cathode should be bigger or equal as anode and insoluble in electrolyte. Anode and cathode
are closely placed to form uniform field. Once the power supply is turned on, the electric field between anode and cathode initiated the electron transport from surface of cathode to anode via electrolyte medium. During this time, the oxygen ions (O$^{2-}$) migrate into anode metal and forms metal-oxides.

After the development of electron microscopy, the porous and barrier type anodic structures are classified. While anodization, the barrier type oxide is formed if the resultant anodic oxide is insoluble in the electrolyte [Diggle et al., 1969]. However if resulting anodic oxide is soluble in electrolyte, it results porous anodic structures. Cross section schematic of these structures are shown in Fig. 2.7. Barrier type and porous type anodic oxides have been intensively investigated for colouring of metal layers [Tanabe et al., 2003], surface protection [Thieme et al., 2003], corrosion resistance [Hou and Chung, 1997], gas sensors [Rani et al., 2013, Kimura et al., 2013] and thin film capacitors [Rosztoczy and Read, 1969, Gupta et al., 2002].

In 1965, C. G. Thornton had reported the various new possibilities in microelectronics fabrication, among which anodization was promising for thin metal-oxide, particularly Al$_2$O$_3$ and Ta$_2$O$_5$ [Thornton, 1965]. Later, few authors have reported fabrication and electrical properties of anodic oxides capacitors for microelectronics [Morley and
Figure 2.7: Schematic view of cross section and SEM images (a) Barrier type (b) Porous type anodic oxides

Campbell, 1973, Ajit and Jawalekar, 1976, Gupta et al., 2002, Hourdakis and Nassiopoulou, 2010, 2012. Jawalekar et al and Wyatt et al were demonstrated the fabrication of Al₂O₃ and Ta₂O₅ capacitors using anodization, respectively [Ajit and Jawalekar, 1976, Wyatt, 1975]. Those thin film capacitors showed less sensitivity of capacitance with frequency and temperature. It was reported that the anodization controls the thickness of dielectric layer precisely with low defect [Ajit and Jawalekar, 1976]. However, the limited number of materials can only be anodized. Also electrical breakdown of oxide during anodization was mentioned as a limiting factor [Ajit and Jawalekar, 1976].

A detailed study on incorporating anodic alumina in MOSFET fabrication was reported by M. B. Das et al in 1976 [Raymond and Das, 1976]. It was concluded that anodization is compatible with existing fabrication methods such as thermal oxidation and CVD. In recent days, Hwu et al demonstrated the importance of anodization/reoxidation in various dielectric material processing for microelectronics [Lin and Hwu, 2003, Chen et al., 2004, Huang and Hwu, 2006, Wang and Hwu, 2010]. They demonstrated the low leakage property of anodic alumina of $EOT = 23\AA^o$ with $23\AA^o$ thick SiO₂ for MOS structures, shown in Fig. 2. 7 [Huang and Hwu, 2003]. The anodic alumina shows improved leakage characteristics compared to SiO₂ of same EOT. This is due to improved ionic polarization of anodic alumina which reduced the ionic and thermionic conduction of dielectrics. Recently, few authors reported the fabrication of MIM capacitors with anodic oxides, such as Al₂O₃ [Hickmott, 2005, Hourdakis and Nassiopoulou, 2012] and Ta₂O₅ [Sedghi et al., 2011]. Hourdakis et al were anodized Al using sulfuric acid which results porous alumina.
This capacitor shows a high sensitivity of capacitance with frequency and high VCC ($>1000\text{ppm}/V^2$). This is due to instability in oxide formation during anodization which results high defect density and noncrystalline alumina. Wet anodization of $\text{Ta}_2\text{O}_5$ results barrier type oxide which shows a low leakage current density of $<10\text{nA/cm}^2$ for 5V and high breakdown field of $>4.3\text{MV/cm}$.

Polarization processes involving in formation of capacitance for barrier type anodic oxides was reported by Kosjuk et al [Kosjuk and Odynets, 1997]. It is concluded that deformation and ionic polarizations are dominant in anodic oxides of Al, Ta and Nb. It is also reported that anodic alumina shows a less sensitivity of capacitance with frequency compared to anodic $\text{Ta}_2\text{O}_5$ and $\text{Nb}_2\text{O}_5$ [Kosjuk and Odynets, 1997]. In this thesis, the anodization was utilized to prepare barrier type $\text{Al}_2\text{O}_3$, $\text{TiO}_2$ and bilayer of $\text{TiO}_2/\text{Al}_2\text{O}_3$ for the fabrication of MIM capacitors. Various studies, such as voltage linearity, leakage characteristics and reliability are reported in detail. It was observed that anodization has large potential to solve many problems in nanoelectronics.

### 2.4 Summary

In this chapter, a detailed review of MIM capacitors with various high-$k$ dielectric materials is presented. It gives a comparative observation of performance parameters and limitation
of recent fabrication trends in MIM capacitors. Among high-\(k\) materials, \(\text{Al}_2\text{O}_3\) showed a promising single layer MIM capacitors for analog and mixed signal applications. This is due to large bandgap of \(\text{Al}_2\text{O}_3\), strong ionic polarization and low dependence with temperature. Though \(\text{HfO}_2\) and \(\text{Ta}_2\text{O}_3\) show twice the dielectric constant of \(\text{Al}_2\text{O}_3\), the leakage current density and VCC are high due to stress induced defects and low ionic polarization. Crystalline \(\text{TiO}_2\) shows a very high dielectric constant (\(\varepsilon_r > 100\)). However, due to dominant orientation polarization and structural defects, it exhibits high leakage current density and VCC. \(\text{TiO}_2\) is suggested for DRAM application since it shows a very high capacitance density of more than \(20\text{fF/\mu m}^2\) compared to any metal-oxides of it’s EOT.

These observations indicate that more attention needs in fabrication process to control the defect/trap in bulk and interfaces. It is also found that the migration of metal ions to dielectric due to high temperature fabrication process which reduces the quality of dielectrics. To avoid this, highly stable electrodes like TiN and TaN shall be utilized. However, it gives additional process flow in regular manufacturing process.

A low cost, low temperature and high quality dielectric processing techniques is needed to sort all these issues. From the literature review on anodization, it was clear that anodic oxides have the potential to solve these issues. The inherent nature of anodic oxides, such as improved ionic polarization and low sensitivity with temperature, the high performance MIM capacitors can be achieved to meet the ITRS requirements. With this motivation, the anodic alumina, titania and dielectric stacks are employed in MIM capacitors in this thesis. Various studies on electrical and structural properties are reported with various characterization techniques in next chapters in detail.