ABSTRACT

Rapid advances in semiconductor technologies have led to a dramatic increase in the complexity of Very Large Scale Integration (VLSI) circuits. With fabrication technology entering deep submicron era, devices are scaled down, more functionalities are integrated into one chip, and chips run at higher clock frequencies. Due to the increasing high complexity of modern chip design, VLSI Computer Aided Design (CAD) tools are important for delivering high system performance and there is a requirement for design automation tools. Thus careful up-front design planning and analyzing physical implementation effects before the actual layout is essential in designing today’s multi-million gate Integrated Circuits (ICs).

Most of the problems in VLSI physical design process are Non-Deterministic Polynomial time (NP) hard problem. The future tremendous growth of VLSI circuits will rely on the development of physical design automation tools. In the physical design process, Floorplanning is an important step, as it sets up the ground work for a good layout. It is the problem of placing a set of circuit modules on a chip to minimize the total area and interconnect cost. Various aspects of VLSI floorplanning problem have been studied in this thesis.

From the literature survey, it has been found that there are three important issues present in floorplanning problems namely i) Performance driven VLSI Floorplanning with and without Constraints ii)
Dimensional (3-D IC) VLSI Floorplanning Representation iii) Thermal Driven VLSI floorplanning.

The first objective of this thesis is to focus on computation time complexity and solution space for VLSI floorplanning problem. This approach is based on B*tree representation using Differential Evolutionary algorithm (DE) which optimizes both chip area and total wire length without overlaps in VLSI macro cell placement. DE algorithm invoked to create new offspring from parent chromosomes instead of classical crossover or mutation due to differential operators. Experimental results show that DE can quickly produce optimal solutions for Microelectronics Center of North Carolina (MCNC) benchmark circuits.

The second objective of this thesis is to present a novel Differential Evolutionary algorithm based on B^Tree representation with placement constraints. It addresses the problem of handling alignment constraints which arises in bus structure. It also deals with performance constraint such as bounded net delay to minimize total wire length. Our approach generates a good placement solution with an optimum area and a short run time. The major advantage using DE is the reduction of computation time by proposing a trial solution (with all constraints) which will not need to evaluate the objective function every time.

The third objective of this thesis is to analyze and categorize some state-of-the-art 3-D representations, and propose a Ternary tree (T-tree) model for 3-D nonslicing floorplans by extending the B*tree from 2D. This work
proposes a novel optimization algorithm for packing of 3D rectangular blocks. The proposed Differential Evolutionary algorithm (DE) is very fast in that it evaluates the feasibility of a Ternary tree (T-tree) representation.

Final objective of this thesis is to redistribute the temperature inside the chip by arranging the blocks in the 2-D rectangular floorplan structure. Here Hotspot, a freeware tool is used to calculate the maximum temperature of the floorplan and use the maximum temperature as one of the objective function in temperature driven floorplanning. Thermal aware floorplanning makes use of the Hybrid Simulated Annealing algorithm (HSA) to reach a globally optimal solution. Experimental result shows that the average and peak temperature is reduced in VLSI circuit modules.