CHAPTER 6

CONCLUSION AND FUTURE WORK

The existing challenges and limited solutions to the different issues under VLSI floorplanning problem include placing a set of circuit modules on a chip to minimize the total area and interconnect cost. And adding constraints such as alignment and performance blocks will make the floorplanning problem more critical. Also, more packing density of the modules inside the floorplanning will lead to increase the temperature and interconnection problem. All these issues must be addressed fully for the successful deployment of the intelligent VLSI floorplan representation. In this thesis an attempt is made to address these issues by proposing robust algorithms and validating them with the MCNC benchmark circuits.

In the first step, a novel DE algorithm based on B*-tree representation has been proposed for non-sliceable floorplanning problem. This thesis discusses on the various optimization algorithms by using the well known topological representation of B* tree. From the comparison results of different algorithms with our proposed algorithm using MCNC benchmarks, it is clear that the DE algorithm shows the better optimized results in the area and computational time.

As a second step, it is proposed that an efficient and effective DE algorithm for floorplanning is based on B*-tree representation with alignment and performance constraints. The proposed DE algorithm guarantees a feasible placement solution with alignment constraints and generates a good
placement with performance constraints during each operation. The advantage of using DE is the reduction of computation time by proposing a trial solution (with all constraints) which does not need evaluating the objective function every time.

As a third step, the thesis has extended towards the three dimensional (3-D) floorplan designs and identified that the floorplanning problem plays a significant role in the 3-D IC Design. So, the concentration on the 3-D ICs floorplanning with DE optimization algorithm is based on T-Tree representation. The proposed DE optimization method dedicates more time to explore the solution space, resulting in better solution and less quality running time. The experimental result shows that it can produce an optimal solution without overlapping each other in the 3-D VLSI floorplanning.

Furthermore, a novel thermal aware floorplanning method using a HSA algorithm has been implemented. The optimized floorplan is obtained and separates available two hot modules to decrease the overall die temperature. It was found out that adding a temperature factor to the objective function does not affect the floorplanning process as a whole. Thus, thermal aware floorplanning can be used as one of the effective methods to reduce the maximum temperature inside the chip.

In VLSI floorplanning, many issues are still open and deserve for further research, especially in the nanometer regime. The future scope of this research work is to apply DE algorithm to the floorplanner using B*-tree representation with floorplanning constraints such as boundary constraints and range constraints to improve the overall performance of the Integrated circuits.

We can also develop a hybrid DE algorithm that relies on the B*-tree representation of 2-D floorplan and T-tree representation for 3-D
floorplanning. The next research direction is that how to make 3-D floorplanning both temperature-aware and leakage-aware is a good topic. One possible approach to achieve this might be adding the leakage power as the fourth term in the objective function of the floorplanner.