ABSTRACT

The increase in demand of portable devices makes Low power device design and it becomes an important field of research. Power dissipation is one of the fundamental design objectives in integrated circuit, after speed. Design of low area, delay and power forms the largest systems in VLSI system design. These three parameters i.e. power, area and speed are always traded off. However, area and speed are usually conflicting constraints, so that improving speed results mostly in larger areas.

The addition and multiplication of two binary numbers are the fundamental and most frequently used arithmetic operation in microprocessors, digital signal processors, and data-processing application-specific integrated circuits. In Multiplier – Accumulator unit addition and multiplication forms the main blocks. High speed and low power MAC units are required for applications of digital signal processing like Fast Fourier Transform, Finite Impulse Response filters, convolution etc. Area and speed of MAC unit are the most significant factors, but sometimes, increasing speed also increases the power consumption, so there is an upper bound of speed for a given power criteria.

Since the various filter designs found in the Digital Signal Processing applications, require computationally efficient multiply and

Accumulate operations so the blocks with the desired characteristics have to be chosen carefully. The target of this thesis is to design and analysis various adder and multiplication schemes for high-speed, area efficient and low power operation Multiplier – Accumulator unit.

This research work will focuses on analyzing a variety of techniques that increases the speed of multipliers and adders as well as reducing the area and power among that suitable one, which is used for Multiplier and Accumulator (MAC) design. This study also illustrates the comparison of various VLSI architectures on the basis of Speed, Area and Power of different type of Adders like Carry Look Ahead Adder, Carry Skip Adder, and Carry Select Adder and the multipliers such as Array Multipliers, Wallace tree multiplier, Booth Encoded Wallace, modified booth multiplier. Then the MAC Unit with Carry Look Ahead Adder, Carry Skip Adder, and Carry Select Adder is designed in which the multiplication is done using the pipelined Modified Booth Encoded Wallace Tree Multiplier to increase the speed, efficiency and for reducing the power. All Adders and Multipliers are described in Verilog and synthesized using Xilinx Spartan-3E trainer kit.

Multipliers are one of the most important parts in signal processing or other computationally intensive applications. Therefore, designing multipliers that are high-speed, low power, and/or regular in layout are of substantial research interest. Many attempts have been made to reduce the number of partial products generated in a multiplication process by using the modified Booth algorithm. Moreover, Wallace Tree CSA structures have been used to sum the partial products in reduced time. By the way, when both

algorithms are combined in one multiplier, a significant reduction in computing multiplications can be expected. The main aim of this project is to reduce the computation time by using Booth's algorithm for multiplication and to reduce chip area by using Carry Save Adders arranged in a Wallace tree structure. For an array multiplier, the computation of the sum bit from an adder cell may also be on the critical path. In this project, Booth Encoded Wallace-tree multiplier is used.

There have been many algorithms application in literature to perform accumulation multiplication, each offering different advantages and having trade-offs in terms of speed, circuit complexity, area and power consumption. In this thesis, a new architecture for a high-speed MAC is designed in which, the computations of multiplication and accumulation are combined and a hybrid-type CSA structure is used to reduce the critical path and improve the output rate. It uses Modified Booth's Algorithm and it is based on 2's complement number system. A modified array structure for the sign bits is used to increase the density of the operands. A carry look-ahead adder (CLA) is inserted in the CSA tree to reduce the number of bits in the final adder. It has been found that Booth Wallace multiplier is the most efficient among all by giving optimum delay, power and area for multiplication.

Then the 8-tap FIR filter is implemented with the proposed MAC unit using Virtex-4 FPGA board. The Virtex-4 board is used since it has more number of DSP slices.