

REFERENCES

1. Abdelgawad, A 2013, 'Low Power Multiply Accumulate (MAC) unit for future wireless networks', Sensors Applications Symposium (SAS), IEEE, pp. 129-132.
2. Abdelgawad, A, & Bayoumi, M 2007, 'High Speed and Area-Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications', IEEE International Symposium on Circuits and Systems, pp. 3199-3202.
3. Asadi, P & Navi, K 2007, 'A new low power 32×32- bit multiplier', World Applied Sciences Journal, vol. 2, no. 4, pp. 341-347.
4. Bui, HT, Wang, Yuke & Jiang, Y 2002, 'Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates', IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 49 , no. 1, pp. 25-30.
5. Chan, PK, Schlag, MDF, Thomborson, CD & Oklobdzija, VG 1991, 'Delay Optimization of Carry - skip Adders and Block Carry-lookahead Adders', proceedings, IEEE Symposium on Computer Arithmetic,
6. Chandrakasan, A, Bowhill, WJ & Cox, FF 2001, 'Design of High-Performance Microprocessor Circuits', IEEE Press, Piscataway.
7. Chandrakasan, A, Sheng, S & Brodersen, R 1992, 'Low-power CMOS digital design', IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484.
8. Chang, CH, Gu, J, & Zhang, M 2005, 'A review of 0.18-μm full adder performances for tree structured arithmetic circuits', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 6, pp. 686-695.
9. Chen, KH, & Chu, YS 2007, 'A Low Power Multiplier With the Spurious Power Suppression Technique', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15 , no. 7, pp. 846-850.

10. Chen, Oscar, TC, Wang, S & Wu, YW 2003, 'Minimization of switching activities of partial products for designing low-power multipliers', *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, pp. 418-433.
11. Chen, OTC, Sheen, RRB & Wang, S 2002, 'A low-power adder operating on effective dynamic data ranges', *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 4, pp. 435-453.
12. Cheng, C & Parhi, KK 2007, 'Low-Cost Parallel FIR Filter Structures With 2-Stage Parallelism[J]', *IEEE Transactions on Circuits and Systems I:Regular*, vol. 54, no. 2, pp. 280 -290.
13. Ching, YN 2005, 'Low-power high-speed multipliers', *IEEE Transactions on Computers*, vol. 54, no. 3, pp. 355-361.
14. Cieplucha, M 2013, 'High performance FPGA-based implementation of a parallel multiplier-accumulator', *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, pp. 485-489.
15. Deepak, S & Kailath, BJ 2012, 'Optimized MAC Unit design', *IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, pp. 1-4.
16. Economakos, G, Bekiaris, D, & Pekmestzi, K 2010, 'A mixed style architecture for low power multipliers based on a bypass technique', *5th International Conference on Design and Technology of Integrated Systems in Nano scale Era (DTIS)*, pp. 1-6.
17. Elguibaly, F 2000, 'A fast parallel multiplier-accumulator using the modified Booth. Algorithm', *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, pp. 902-098.
18. Fayed, A, Elgharbawy, W & Bayoumi, M 2004, 'A merged multiply accumulate for high-speed signal processing application', *ICASSP IEEE*.
19. Fayed, Ayman, A, Bayoumi & Magdy, A 2002, 'A Merged Multiplier-Accumulator for high speed signal processing applications', *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, pp. 3212-3215.

20. Goel, S, Kumar, A & Bayoumi, MA 2006, 'Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style', IEEE Transactions on Very Large Scale Integration Systems, vol. 14, no. 12, pp. 1309-1321.
21. Hernandez, MA & Aranda, ML 2011, 'CMOS Full-Adders for Energy-Efficient Arithmetic Applications', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 4.
22. Hoang, TT, Sjalander, M & Edefors, LP 2010, 'A High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit', IEEE Transactions on Circuits and systems, no. 12, pp. 3073-3081.
23. Hsun, L, Chen, C, Chen, LHC, Kwon, O, Nowka, K & Swartzlander, EE 2000, 'A 16-bit x 16-bit MAC design using fast 5:2 compressors', Proceedings of IEEE International Conference on Application Specific Systems, Architectures, and Processors, pp. 235-243.
24. Huang, Z, & Ercegovac, MD 2005, 'High-performance low-power left-to-right array multiplier design', IEEE Transactions on Computers, vol. 54, no. 3, pp. 272-283.
25. Hussin, R, Shakaff, AYM, Idris, N, Sauli, Z, Iismail, RC & Kamarudin, A 2008, 'An efficient modified Booth multiplier architecture', International Conference on Electronic Design, 978-1-4244-2315-6/08, IEEE.
26. Hwang, S, Han, G, Kang, S, Kim, J 2004, 'New Distributed Arithmetic Algorithm for Low-Power FIR Filter Implementation', IEEE Signal Processing Letters, vol. 11, no. 5, pp. 463-466.
27. Hwang, YZ, Lin, JF, Sheu, M & Sheu, CJ 2007, 'Low Power Multipliers Using Enhanced Row Bypassing Schemes', IEEE Workshop on Signal Processing Systems, pp. 136-141.
28. Jaina, D, Sethi, K & Panda, R 2011, 'Vedic Mathematics Based Multiply Accumulate Unit', International Conference on Computational Intelligence and Communication Networks (CICN), pp. 754-757.
29. Khouja, N, Grati, K & Ghazel, K 2007, 'Low Power implementation of Decimation Filters in Multistandard Radio Receiver Using optimized Multiplication-Accumulation Unit', IEEE Publications.

30. Kim, S & Cho, K 2010, 'Design of high-speed modified Booth multipliers operating at GHz ranges', World Academy of Science, Engineering and Technology.
31. Ko, U, Balsara, PT & Lee, W 1995, 'Low-power design techniques for high-performance CMOS adders', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 3 , no. 2 , pp. 327-333.
32. Kodek, DM 2005, Performance limit of finite word length FIR digital filters, IEEE Trans. Signal Processing vol. 53, pp. 2462-2469.
33. Liao, MJ, Su, CF, Chang & Wu, A 2002, 'A carry select adder optimization technique for high-performance Booth-encoded Wallace tree multipliers', IEEE International Symposium on Circuits and Systems.
34. Liu, D & Svensson, C 1993, 'Trading speed for low power by choice of supply and threshold voltages', IEEE Journal of Solid-State Circuits, vol. 28, no. 1, pp. 10-17.
35. Longa, Patrick & Miri, A 2006, 'Area-Efficient FIR Filter Design on FPGAs using Distributed Arithmetic', IEEE International Symposium on Signal Processing and Information Technology, pp. 248-252.
36. Mangal, SK, Badghare, RM, Raghavendra, B, Deshmukh & Patrikar, RM 2007, 'FPGA Implementation of Low Power Parallel Multiplier', IEEE Publications.
37. Mehendale, M, Sherlekar, SD & Venkatesh, G 1998, 'Low-Power Realization of FIR Filters on Programmable DSP's', IEEE Transactions on Signal Processing, pp. 546-553.
38. More, TV & Kshirsagar, RV 2011, 'Design of low power column bypass multiplier using FPGA', 3rd International Conference on Electronics Computer Technology (ICECT), vol. 3, pp. 431-435.
39. Narayanan, GL & Venkataramani, B 2005, 'Optimization techniques for FPGA -based wave pipelined DSP blocks', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 3, no. 7, pp.783-792.

40. Nikolaidis, S, Karaolis, E & Bitzaros, EDK 1999, 'Estimation of the transition activity in MAC architectures implementing FIR filters', Proceedings of ICECS, The 6th IEEE International Conference on Electronics, Circuits and Systems, vol. 2, pp. 919-923.
41. Oscar, TC, Wang, S, Wu, YW & Chen, 2003, 'Minimization of switching activities of partial products for designing low-power multipliers', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 3, pp. 418-433.
42. Pacheco, BD & Linares, AM 2004, 'A low power and high speed CMOS voltage-controlled ring oscillator', IEEE International Symposium on Circuits and Systems ISCAS, no. 4, pp. 752-755.
43. Panato, A, Silva, S, Wagner, F, Johann, M, Reis, R & Bampi, S 2004, Design of very deep pipelined multipliers for FPGAs, Proceedings of the Design, Automation and Test in Europe Conference and Exhibition Designers Forum, pp.1530-1591.
44. Piguet, C 2007, 'Low power design in deep submicron 65 and 45 nm technologies', ICECS 2007 pp. 915-918,
45. Rabaey, JM & Pedram, M 1996, 'Low Power Design Methodologies', Kluwer Academic Publisher.
46. Rabaey, JM, Chandrakasan, A & Nikolic, B 2003, Digital Integrated Circuits, A Design Perspective, Prentice Hall, Upper Saddle River, NJ,.
47. Raghunath, RKJ 1997, 'A compact carry-save multiplier architecture and its Applications', Proceedings IEEE 40th Midwest Symposium on Circuits and Systems, vol. 2, pp. 794-797.
48. Ramesh, AP, Tilak, AVN, & Prasad, AM 2012, 'efficient implementation of 16- bit Multiplier-accumulator using radix-2 Modified booth algorithm and spst adder using verilog', International Journal of VLSI Design & Communication Systems (*VLSICS*), vol. 3, no. 3.
49. Ramkumar, B & Kittur, HM 2012, 'Low- Power and Area Efficient Carry Select Adder'IEEE Transactions. On Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 371-374.

50. Rao, PV, Raj, PCP & Ravi, S 2009, 'VLSI Design and Analysis of Multipliers for Low Power', IEEE Conference Publications, Fifth International Conference on Intelligent Information Hiding and Multimedia Signal Processing, pp. 1354-1357.
51. Rashidi, B & Pourormazd, M 2011, 'Design and implementation of low power Digital FIR Filter based on low power multipliers and adders on Xilinx FPGA', IEEE Publications.
52. Saravanan, S & Madheswaran, M 2010, 'Modified Multiply and Accumulate Unit with Hybrid Encoded Reduced Transition Activity Technique Equipped Multiplier and Low Power 0.13 μ m Adder for Image Processing Applications' International Journal of Computer Applications, vol. 1, no. 9.
53. Schulte, MJ, Balzola, PI, Akkas, A & Brocato, RW 2000, 'Integer Multiplication with Overflow Detection or Saturation', IEEE Transactions on Computers, vol. 49, no. 7.
54. Seo, YH & Kim, D 2010, 'A New VLSI Architecture of Parallel Multiplier Accumulator Based on Radix-2 Modified Booth Algorithm', IEEE transactions on very large scale integration (VLSI) system, vol. 18, no. 2.
55. Shams, AM, Darwish, TK & Bayoumi, MA 2002, 'Performance analysis of low-power 1-bit CMOS full adder cell', IEEE Transactions on Very Large Scale Integration Systems (VLSI), vol. 10, no. 1, pp. 20-29.
56. Shans, AM, Badawy, WM & Bayomi, MA 1998, 'An Enhanced Low-Power computational kernel for a pipelined multiplier-accumulator unit', Proceedings of the tenth International Conference on Microelectronics ICM.
57. Shanthala, S, Raj, CP & Kulkarni, SY 2009, 'Design and VLSI Implementation of Pipelined Multiply Accumulate Unit', 2nd International Conference on Emerging Trends in Engineering and Technology (ICETET), pp. 381-386.
58. Shen, NY, Chen & Oscar, TC 2002, 'Low-power multipliers by minimizing switching activities of partial products', IEEE International Symposium on Circuits and Systems, ISCAS, vol. 4, pp. 93-96.

59. Shin, K, oh, IK, Min, S, Ryu, BS, Lee, KY & ChoT, W 1999, 'A Multi-Level Approach to Low Power Mac Design' IEEE Transactions on VLSI systems, vol. 48, no. 3, pp. 361-763.
60. Sinha, D, Sharma, T, Sharma, KG & Singh, BP 2011, 'Design and Analysis of low Power 1-bit Full Adder Cell', IEEE.
61. Sklanski, J 1960, 'Conditional-sum addition logic', IRE Transaction on Electronic Computers, vol. 9, pp. 226-231.
62. Song, PJ, & Micheli, DG 1991, 'Circuit and architecture trade-offs for high-speed multiplication', IEEE Journal of Solid-State Circuit, vol. 26, no. 9, pp. 1184-1198.
63. Sulistyo, JB & Ha, DS 2003, '5 GHz Pipelined multiplier and MAC in 0.18 μ M Complementary Static CMOS', International Symposium on circuits and systems, pp. 371-374.
64. Tsao, TC & Choi, K 2012, 'Area-Efficient Parallel FIR Digital Filter Structures for Symmetric Convolutions Based on FIR Algorithm', IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 399-371.
65. Unsal, OS & Koren, I 2003, 'System-level power-aware design techniques in real time systems', Proceedings Of The IEEE, vol. 91, no. 7, pp. 1055-1069.
66. Veendrick, H 1984, 'Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits', IEEE Journal of Solid-State Circuits, vol. 19, no. 4, pp. 468-473.
67. Vesterbacka, M 1999, 'A 14-transistor CMOS full adder with full voltage-swing nodes', IEEE Workshop on Signal Processing Systems, pp. 713-722.
68. Vinod, AP & Lai, EMK 2005, 'On the implementation of efficient channel filters for wideband receivers by optimizing common sub expression elimination methods', IEEE Trans. Computer-Aided Design Integr. Circuits Syst., vol. 24, no. 2, pp. 295-304.
69. Wallace, CS 1964, 'A suggestion for a fast multiplier', IEEE Transactions on Electronic Computers, vol. 13, pp. 14-17.

70. Wen, MC, Wang, SJ & Lin, YN 2005, 'Low power parallel multiplier with column bypassing', IEEE Conference Publications, IEEE International Symposium on Circuits and Systems, vol. 2, pp. 1638-1641.
71. Yoo, H, & Anderson, DV 2005, 'Hardware-Efficient Distributed Arithmetic Architecture For High-order Digital Filters, IEEE International Conference on Acoustics, Speech and Signal Processing, vol. 5, pp. 125-128.
72. Yue, Q, Zhancai, LI & Qin, W 2005, 'Low-Power Fir Filter Based on Standard Cell", IEEE Publications'.
73. Zhu, N, Goh, WG, Zhang, W, Yeo, KS & Kong, ZH 2010, 'Design of Low-Power High-Speed Truncation-Error-Tolerant Adder and Its Application in Digital Signal Processing', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 8.