CHAPTER 6

CONCLUSION AND FUTURE WORK DIRECTIONS

6.1 CONCLUSION

The general conclusion drawn from this thesis and some suggested new directions are presented in this paper. The objective of this thesis is to design suitable low power MAC unit for FIR filters. This thesis investigates and examines fast adder and multiplication schemes, and utilizes them in the design and implementation of a MAC unit. A low power, area efficient and high speed 16 × 16 bit MAC unit have been presented in this paper. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. The designs of various adders and multipliers have been implemented on FPGA board using Spartan- 3E XC3S500E, PQ208 trainer kit using Xilinx 13.2 software and Xilinx ISIM simulator for simulation.

A study has been made on different techniques for low power and efficient adders and multipliers for MAC unit. From the study, the pipelining technique is used for proposed MAC unit, where its adder and multiplier for partial product generation and it has been synthesized and analyzed. Further, comparison of different adders and multipliers are done on various performance measures. Discussions made in adder topologies illustrate that the carry select adder among all the adders are having the optimized power and delay, with increase in smaller area. Carry select adder has comparatively low value of critical path length, hence less combinational path delay but it

has higher number of leaf cell count and combinational path area. From multiplier topologies modified booth encoded Wallace tree multiplier is analyzed as the optimized one, as there is a tradeoff between area, delay and power.

The pipelining is the most widely used technique to improve the performance of digital circuits. By employing the pipelining technique for proposed MAC unit the speed increases by the factor of 50% with penalty on area increasing by factor of 1%. It is concluded that pipelining improves performance of multiplier although; speed improvement ratio is superior to the area increase ratio. Comparisons are based on the synthesis reports keeping one common base for comparison specifically, the same FPGA device with same design constraints disguised for the synthesis of each adder, multiplier and MAC unit.

Design for low power FIR filter using proposed MAC unit has been presented in this paper. The 8 tap FIR Filter is implemented with proposed MAC unit on Virtex-4 board. The power reduction is achieved through the usage of a proposed MAC unit inside the filters that reduce the total activity and the dynamic power. This approach gives a better performance than the common filter structures in terms of speed of operation, efficiency and power consumption.

6.2 DIRECTIONS FOR FUTURE RESEARCH

At different abstraction level, a detailed power calculation can be done using Prime power and hence possibility of power reduction at different abstraction level can be considered. Furthermore, a trade-off between area, speed and power can be brought satisfying power constraint. ASIC design for the low power digital filter with low power latch and clock gating can be carried out.