CHAPTER 5

MULTIPLY AND ACCUMULATE UNIT FOR DIGITAL FILTERS

5.1 INTRODUCTION

Digital filters are the most frequently used elements in signal processing applications. Among digital filters, FIR filters are preferred due to their stability, easily achievable linear-phase property, and low quantization word length sensitivity. All these desirable properties come with a drawback compared to their recursive counterparts IIR filters: increased computational workload, hence power. This, in turn, leads to excessive amount of power dissipation which is a bottleneck for today's low power demanding applications.

In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit consumes low power and is always a key to achieve a high performance digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications. This chapter is to analyze optimized area and delay MAC unit for FIR filter.

5.2 FIR FILTERS

Digital filters can be divided into two categories: finite impulse response (FIR) filters; and infinite impulse response (IIR) filters. In general,

FIR filter requires higher taps than IIR filters to obtain similar frequency characteristics, FIR filters are widely used because they have linear phase characteristics, guarantee stability and are easy to implement with multipliers, adders and delay elements as discussed by Kodek (2005). The number of taps in digital filters varies according to applications. In commercial filter chips with the fixed number of taps , zero coefficients are loaded to registers for unused taps and unnecessary calculations have to be performed. To alleviate this problem, the FIR filter chip provides variable-length taps have been widely used in many application fields. However, these FIR filter chips use memory, an address generation unit, and a modulo unit to access memory in a circular manner. Vinod et al (2005) proposes two special features called a data reuse structure and a recurrent-coefficient scheme to provide variable-length taps efficiently. Since the proposed architecture only requires several MUXs, registers, and a feedback-loop, the number of gates can be reduced over 20 % than existing chips.

In general, FIR filtering is described by a simple convolution operation as expressed in the Equation 5.1

$$y[n] = \sum_{k=0}^{N-1} h[k].x[n-k] \tag{5.1}$$

where x[n], y[n], and h[n] represent data input, filtering output, and a coefficient, respectively and N is the filter order. The equation using the bit-serial algorithm for a FIR filter and it is represented in Equation 5.2

$$y[n]= \sum_{k=0}^{N-1} \sum_{j=0}^{M-1} \left(h_j[k].2^j\right).x[n-k] \tag{5.2}$$

where the hj, N and M are the jth bit of the coefficient

5.3 MULTIPLY AND ACCUMULATE UNIT

In chapters 3 and 4, adders and multipliers are analyzed and comparison is made on the basics of power consumption, area and delay. From the analysis, the Carry select adder and Modified Booth Encoded Wallace tree multiplier is chosen for proposed MAC unit. The Figure 5.1 shows the MAC unit with selected adders and multipliers.

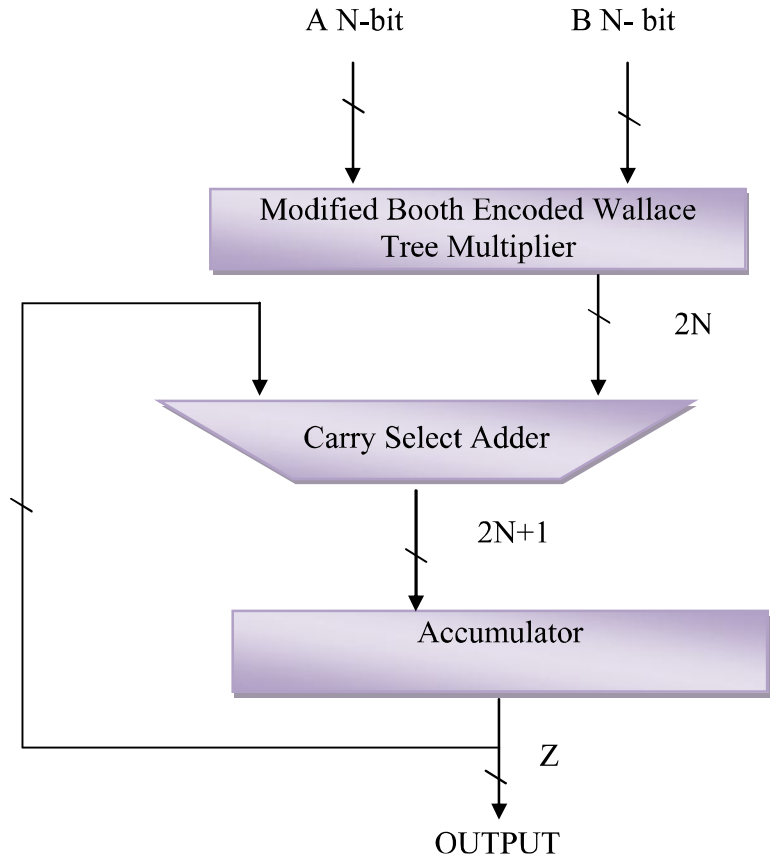

Figure 5.1 MAC unit with proposed adder and multiplier

The MAC unit is divided into three pipe stages so they have the ability to be clocked at a faster rate. The latency is three cycles for a MAC or multiply instruction, but the throughput is one operation per cycle. Figure 5.1 shows a block diagram of the MAC unit with the proposed adder and multiplier. The first pipe stage is for generating the partial products and the

second pipe stage continues accumulation of the partial products The third and final pipe stage contains accumulator to complete the MAC. This stage is the critical pipeline stage of the MAC unit. For the accumulator the adder is to be chosen and it gives optimized power, area and delay. The selected adder and multiplier combination is synthesized with other adder for analyzing, whether the selected adder and multiplier combination with a adder for accumulator is best among all the adders with proposed adder and multiplier combination.

The Table 5.1 gives the comparison of different adders with selected adder and multiplier combination for MAC unit. From the comparison, the MAC unit is selected with area efficient, low power and delay.

Table 5.1 Comparison of different adders with selected adder and multiplier combination

MAC	Area	Delay	Power Dissipation
Modified Booth Encoded Wallace tree Multiplier and Carry select adder Combination with Block Carry look ahead adder (MAC 1)	6%	35.46	85.83
Modified Booth Encoded Wallace tree Multiplier and Carry select adder with carry look ahead adder (MAC 2)	6%	41.53	84.99
Modified Booth Encoded Wallace tree Multiplier and Carry select adder combination with carry select adder (MAC 3)	6%	33.53	85.28
Modified Booth Encoded Wallace tree Multiplier and carry select adder combination with fixed block size carry skip adder (MAC 4)	6%	41.51	85.31

The analysis is made for different MAC unit by synthesizing the selected adder and multiplier combination with other adders. From the comparison made the area for all the MAC unit is 6% and the power dissipation is nearly same. Then by comparing the delay of each MAC unit, the carry select adder is having the lowest delay among all the adders. So, for accumulation the carry select adder is chosen. Figure 5.2, 5.3 and 5.4 show the graph for the MAC unit comparison based on area, delay and power consumption.

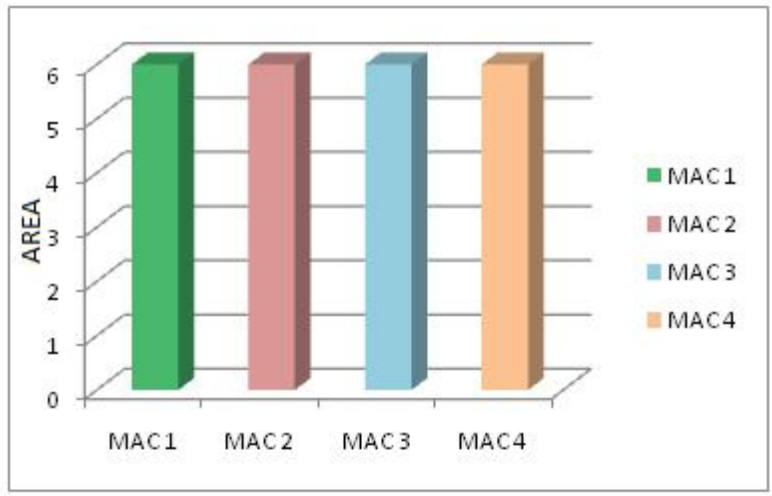

Figure 5.2 Area comparisons of synthesized MAC units

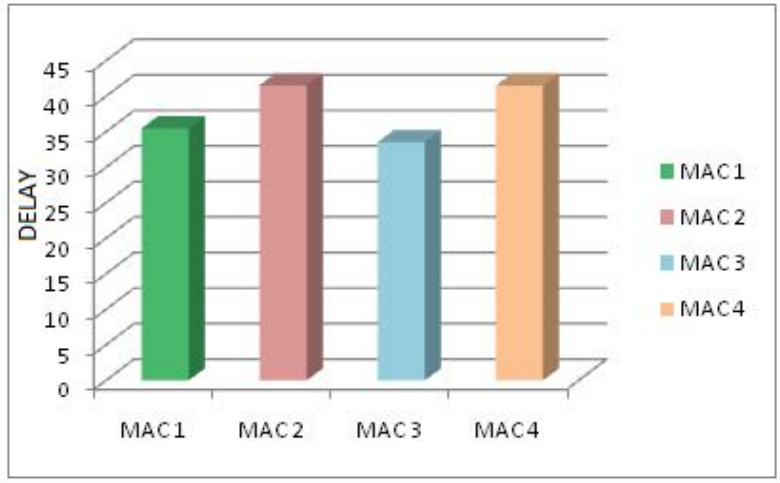

Figure 5.3 Delay comparisons of synthesized MAC units

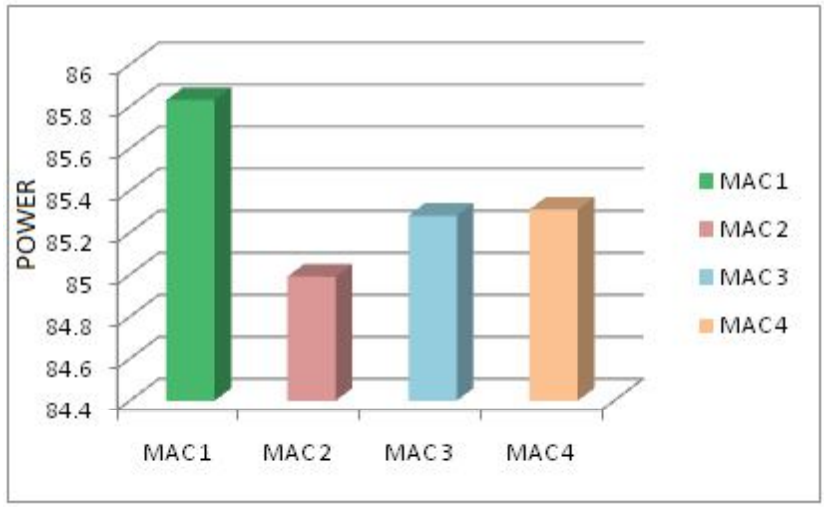

Figure 5.4 Power comparisons of synthesized MAC units

5.4 PROPOSED MAC UNIT

The MAC unit determines the speed of the overall system; it always lies in the critical path. Many researchers have attempted in designing MAC architecture with high computational performance and low power consumption. In order to improve the speed of the MAC unit, there are two major bottlenecks that need to be considered. The first one is the partial products reduction network that is used in the multiplication block and the second one is the accumulator. Both of these stages require addition of large operands that involve long paths for carry propagation.

The carry select adder and Modified booth encoded Wallace tree multiplier is chosen for partial product reduction and for accumulation carry select adder. From the selected adders and multiplier, pipelining is introduced for further reduction in area, power and delay. The Figure 5.5 shows the proposed MAC unit (pipelined MAC unit).

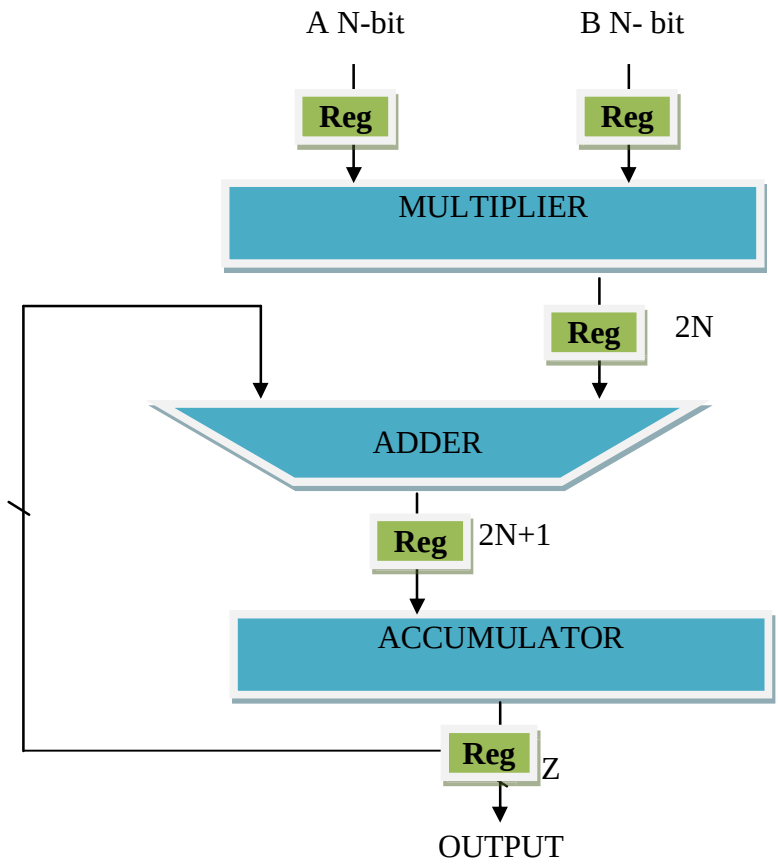

Figure 5.5 Proposed MAC unit

The speed of the MAC unit can further increased by pipelining. The speed of the MAC unit is greatly improved by proper deciding the number of pipeline stages and the positions for the pipeline registers to be inserted as discussed by Sulistyo & Ha (2003). Pipelines are widely used to improve the performance of digital circuits, since they provide a simple way of implementing parallelism from streams of sequential operations. In a pipelining system, the maximum operating frequency is limited by slowest stage which has the longest delay. As more stages are inserted in the pipeline, each stage becomes shorter and ideally presents a smaller delay. Theoretically, the pipeline depth can be pushed to a level of using a single gate between two registers as discussed by Panato et al (2004). But usually,

there is a compromise between performance improvements obtained with increased pipeline depth and the penalties imposed by the additional memory elements inserted in between the stages. So trade-off between the reduction in delay due to pipelining and increase in area must always be considered. The Table 5.2 gives the area, power and delay values after synthesizing the proposed MAC unit with pipelining.

Table 5.2 Proposed MAC unit – area, delay and power dissipation values

Proposed MAC unit	Lut	Delay	Power
	7%	15.392 ns	74.19 mW

By employing pipelining, speed increases by the factor of 2.1 with penalty on area increasing by factor of 0.85. However, speed improvement ratio is larger than the area increase ratio, it is concluded that pipelining improves performance of MAC unit. Power dissipation also reduces by a factor of 0.89.All comparison for adders, Multipliers and MAC unit is based on the synthesis reports keeping one common base for comparison. That means the same FPGA device is targeted (part number and speed grade) with same design constraints implied for the synthesis of each multiplier. The output waveform for the proposed MAC unit is shown in Figure 5.6.

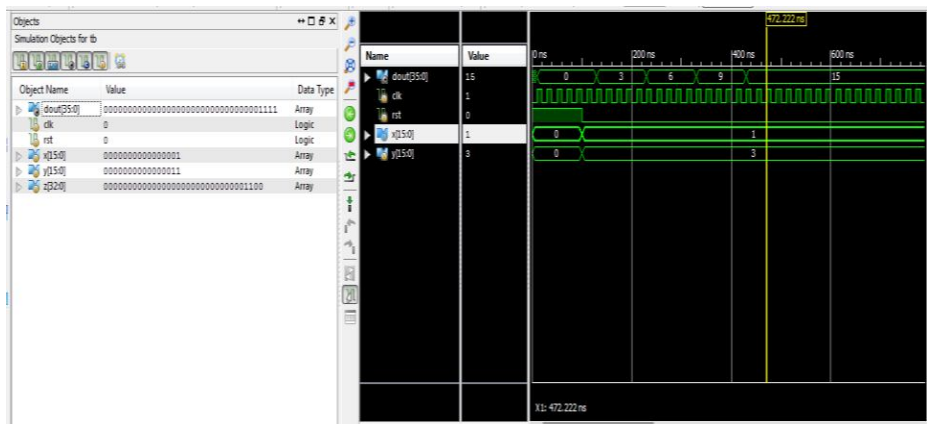

Figure 5.6 Simulation output of proposed MAC unit

5.5 PROPOSED MAC APPLICATION IN FIR FILTER

Finite impulse response (FIR) filters are widely used in various DSP applications.This section describes an approach to the implementation of low power digital FIR filter using proposed MAC unit. For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. Glitches are due to converging combinatorial paths with different propagation delays. Signal glitching refers to the transitory switching activity within a circuit as logic values propagate through multiple levels of combinational logic. Pipelining is a simple and effective way of reducing glitching, and hence minimizing power consumption. It is found that, at a given clock speed, pipelining can reduce the amount of energy per operation by between 40% and 90% for applications such as integer multiplication, CORDIC, triple DES, and FIR filters. The Figure 5.7 shows the synthesis output of FIR filter with proposed MAC unit and in figure 5.8 the simulated output of 8 tap FIR is shown by constant coefficient on FPGA board..The target board used for simulating and synthesizing the 8 tap FIR filter is Virtex 4.

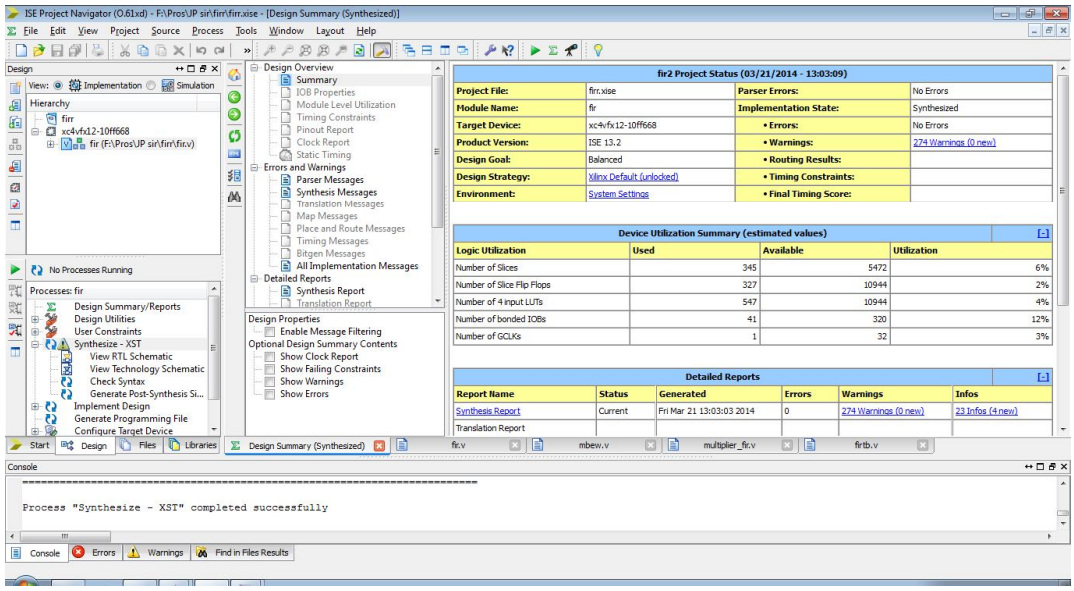

Figure 5.7 Synthesis output for FIR with proposed MAC unit

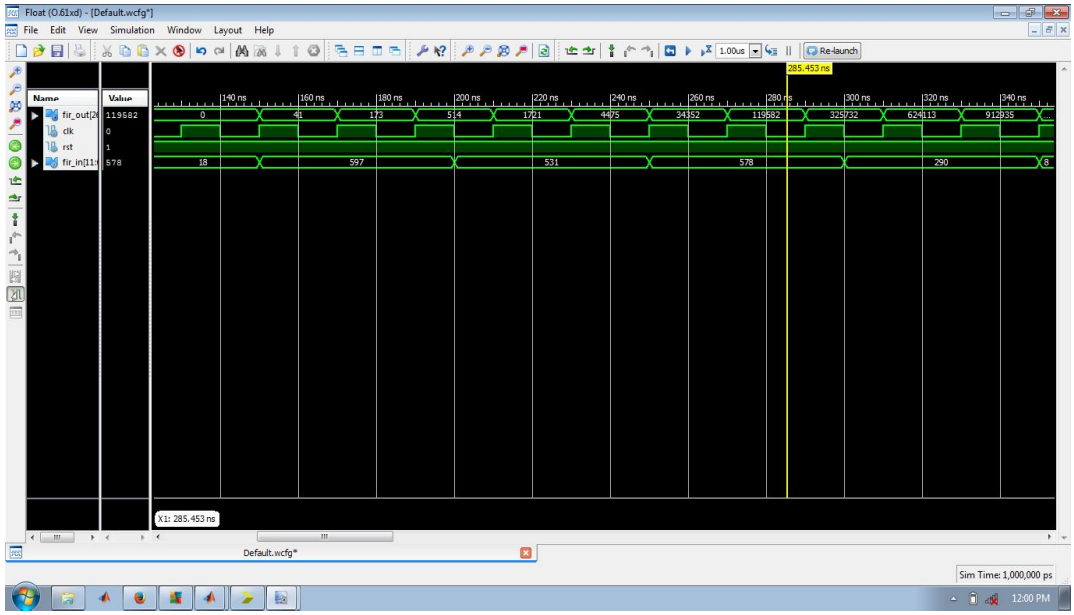

Figure 5.8 Simulation output of FIR filter with proposed MAC unit

The power summary of FIR filter with proposed MAC unit is shown in Figure 5.9 and Floor plan for FIR filter using Virtex – 4 XC4VFX12 is shown in Figure 5.10.

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	14.63	1	---	---
Logic	0.00	544	10944	5
Signals	0.08	738	---	---
IOs	16.88	41	320	13
Quiescent	165.59			
Total	197.17			

Figure 5.9 Power Summary of FIR filter with proposed MAC unit

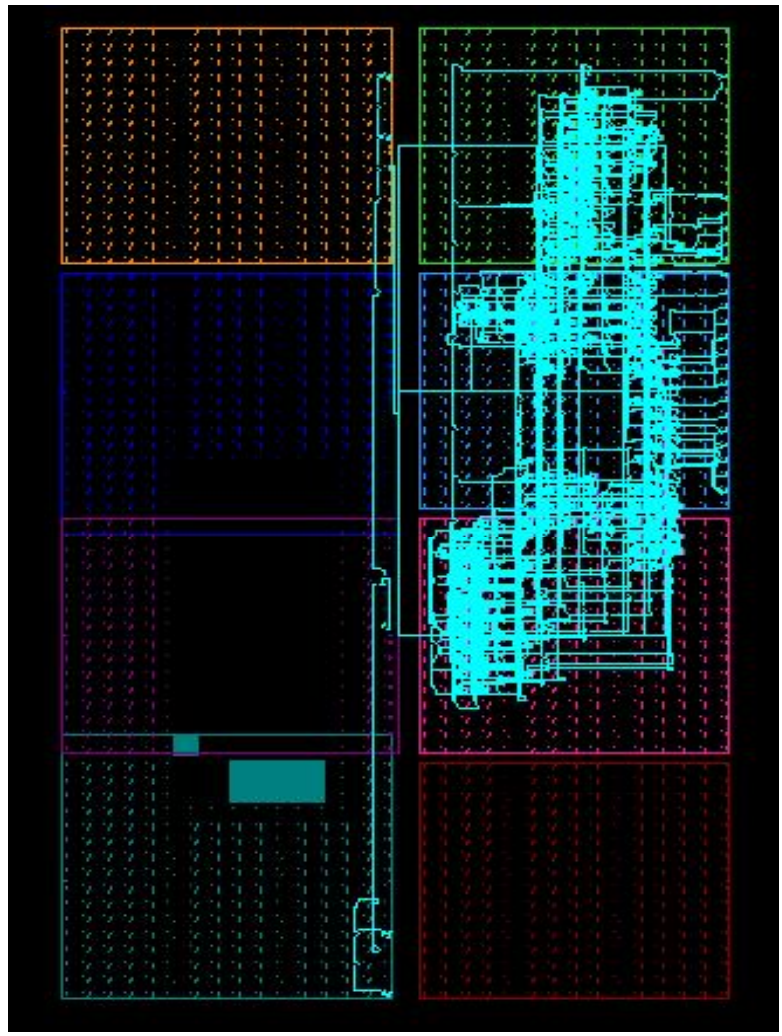

Figure 5.10 FPGA Floor Plan of FIR filter with proposed MAC unit

5.6 CONSLUSION

This chapter discusses about high speed, area efficient and low power MAC unit for FIR filters. Analysis and comparison is made for adders and multipliers and from that MAC unit is designed using carry select adder and Modified booth encoded Wallace tree multiplier. The selected adder and multiplier is used for partial product generation and this combination is analyzed with different adders which is to be used for accumulation. In this comparison, the carry select adder gives the optimized output. The proposed MAC is then added with intermediate registers i.e, pipelining. After

pipelining the proposed MAC unit the delay reduces by 50% and 10% reduction in power dissipation. But the area of MAC unit increases by 1%. As the variation in area percentage is very small when compared to speed and power consumption, the proposed MAC unit is concluded as having optimized area, power and high speed. The MAC unit designed in this work is used in 8 tap FIR filter realization for High speed DSP applications on Virtex-4 FPGA board.