CHAPTER 4

COMPARATIVE ANALYSIS OF FAULT TOLERANT MINs BASED ON THE VARIOUS PERFORMANCE FACTORS

4.1 Introduction

The applications of interconnection networks (INs) are the on chip networks, storage area networks, local area networks, wide area networks and many other networks [1-6]. IN provides the connectivity amid various components of a network, e.g. connectivity between processor and memory. Multi-stage interconnection networks (MINs) are the prominent category of INs.

MINs show their eminence since it provides high speed and reliability to all parallel and telecommunication applications. Omega network [16-19], advance omega network [16], and clos network [52] are the well-known example of MINs. In general, there are N inputs and N outputs in a MIN which are connected via a number of switching stages. There are various issues which affect the efficiency of a MIN. In this chapter, the author has considered the issue of fault tolerance since it is the most extensively investigated topic in MINs. It can be understood as follows:

"The basic idea for fault-tolerance is to provide multiple paths between source and destination so that alternate paths can be used in case of faults [22]."

Further, the faulty situations in MINs create problems for the data packets which are to be transmitted from the given source to the given destination. Here the term "faulty situations" refers to the faulty switching elements (SEs) in the network. Further, the data transmission process can be based on following three methods.
• Message unicasting
• Message multicasting
• Message broadcasting

If the data packets are transmitted from a single source to a single destination, then it comes in the message unicasting method. If the data packets are transmitted from a source to an arbitrary number of destinations, then it comes in message multicasting method. If the data packets are transmitted from a source to all given destinations, then it comes in message broadcasting method. In this chapter, the author has applied message broadcasting technique to analyze the performance of proposed MINs.

4.2 Related Work

In this chapter, the author has proposed two new interconnection networks named as irregular advance omega network (IAON) and irregular augmented shuffle exchange network-3 (IASEN-3) and their routing algorithms. The architecture of IAON and IASEN-3 are based on previously proposed advance omega network (AON) [16] and irregular augmented shuffle exchange network-2 (IASEN-2). The author compares the performances of MALN [21], IASEN-2, IAON and IASEN-3 in non-faulty and single switch faulty conditions.

Single switch faulty condition means network has one faulty SE in each stage simultaneously. It has been observed that the IAON is better than the MALN and IASEN-2 in single switch faulty and non-faulty conditions. Further, when it compared with IASEN-3 then it is observed that IASEN-3 produce better results than the IAON. However, IAON shows double switch fault tolerability whereas IASEN-3 shows single switch fault tolerability. Double switch fault tolerant means the network can sustain 2 faulty SEs in each stage simultaneously. Further, the structures and routing algorithms of MALN and IASEN-2 is already discussed in chapter 2 and 3 respectively. In table 4.1 and 4.2, various symbols and their meaning are defined which are used throughout the chapter.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning of Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Alternate SE$_1$</td>
<td>First alternate SE of stage 1</td>
</tr>
<tr>
<td>Second Alternate SE$_1$</td>
<td>Second alternate SE of stage 1</td>
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<tr>
<td>First Alternate SE$_3$</td>
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<td>Primary SE of stage 3</td>
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<tr>
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<td>Faulty</td>
</tr>
<tr>
<td>N</td>
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<tr>
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<tr>
<td>$BW_{IAON}$</td>
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<td>Bandwidth of IASEN-3</td>
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<tr>
<td>$PA_{IAON}$</td>
<td>Probability of acceptance of IAON</td>
</tr>
<tr>
<td>$PA_{IASEN-3}$</td>
<td>Probability of acceptance of IASEN-3</td>
</tr>
<tr>
<td>TT</td>
<td>Transmission Time</td>
</tr>
<tr>
<td>$TT_{1, N_{MALN}}$</td>
<td>TT of MALN of network size N in non-faulty condition</td>
</tr>
<tr>
<td>$TT_{1, N_{IASEN-2}}$</td>
<td>TT of IASEN-2 of network size N in non-faulty condition</td>
</tr>
<tr>
<td>$TT_{1, N_{IAON}}$</td>
<td>TT of IAON of network size N in non-faulty condition</td>
</tr>
<tr>
<td>$TT_{1, N_{IASEN-3}}$</td>
<td>TT of IASEN-3 of network size N in non-faulty condition</td>
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<td>TT of MALN of network size N in faulty condition</td>
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<td>TT of IASEN-3 of network size N in faulty condition</td>
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</tr>
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<td>Throughput of IASEN-2 in non-faulty condition</td>
</tr>
<tr>
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<td>Throughput of IAON in non-faulty condition</td>
</tr>
<tr>
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<tr>
<td>$TP_{\text{faulty}_{IASEN-3}}$</td>
<td>Throughput of IASEN-3 in faulty condition</td>
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Table 4.1 Symbol Table.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning of Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Pi_{MALN}$</td>
<td>Processor utilization of $MALN$ in non-faulty condition</td>
</tr>
<tr>
<td>$\Pi_{IASEN-2}$</td>
<td>Processor utilization of $IASEN-2$ in non-faulty condition</td>
</tr>
<tr>
<td>$\Pi_{IAON}$</td>
<td>Processor utilization of $IAON$ in non-faulty condition</td>
</tr>
<tr>
<td>$\Pi_{IASEN-3}$</td>
<td>Processor utilization of $IASEN-3$ in non-faulty condition</td>
</tr>
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<td>Processor utilization of $MALN$ in faulty condition</td>
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<td>Processor utilization of $IAON$ in faulty condition</td>
</tr>
<tr>
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<td>Processor utilization of $IASEN-3$ in faulty condition</td>
</tr>
<tr>
<td>$\Pi_{MALN}$</td>
<td>Processor power of $MALN$ in non-faulty condition</td>
</tr>
<tr>
<td>$\Pi_{IASEN-2}$</td>
<td>Processor power of $IASEN-2$ in non-faulty condition</td>
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<tr>
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<td>Processor power of $IAON$ in non-faulty condition</td>
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<tr>
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<tr>
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<tr>
<td>$\Pi_{faulty_IASEN-2}$</td>
<td>Processor power of $IASEN-2$ in faulty condition</td>
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<tr>
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<td>Processor power of $IAON$ in faulty condition</td>
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<tr>
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<td>Processor power of $IASEN-3$ in faulty condition</td>
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<td>$SE-a$</td>
<td>Switching element $a$ of the network</td>
</tr>
<tr>
<td>$SE-b$</td>
<td>Switching element $b$ of the network</td>
</tr>
<tr>
<td>$SE-c$</td>
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<tr>
<td>$SE-d$</td>
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<td>$SE-e$</td>
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<td>$SE-f$</td>
<td>Switching element $f$ of the network</td>
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<td>$SE-g$</td>
<td>Switching element $g$ of the network</td>
</tr>
<tr>
<td>$SE-h$</td>
<td>Switching element $h$ of the network</td>
</tr>
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<td>$SE-i$</td>
<td>Switching element $i$ of the network</td>
</tr>
<tr>
<td>$SE-j$</td>
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<tr>
<td>$SE-k$</td>
<td>Switching element $k$ of the network</td>
</tr>
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<td>$SE-m$</td>
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<td>$SE-n$</td>
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<td>$SE-q$</td>
<td>Switching element $q$ of the network</td>
</tr>
<tr>
<td>$SE-r$</td>
<td>Switching element $r$ of the network</td>
</tr>
</tbody>
</table>

Table 4.2. Symbol Table.
4.3 Irregular Advance Omega Network

This section gives a detail description of IAON.

4.3.1 Structure of Irregular Advance Omega Network

Irregular advance omega network is derived from advance omega network [16]. In figure 4.1, the source address, destination address, multiplexer and demultiplexer are represented by S, D, Mux and Demux respectively.

![Diagram of IAON](image)

Figure 4.1.16×16 IAON.

In IAON, every source has connectivity with two SEs of first stage through auxiliary links. Similarly, every destination has connectivity with two SEs of third stage through auxiliary links. The auxiliary links of second stage are shown by dotted lines in figure 4.1. The network has 1 primary and 2 alternate path between every source and destination. If a SE has direct connectivity with any source or destination then it will be known as primary SE. If a SE has connectivity with any source or destination through auxiliary links then it will be named as first and second alternate SE respectively.
Based on this assumption, it is understood that SE a, b and c will be the primary, first alternate and second alternate SEs for source 0, respectively. Similarly, the primary, first alternate, and second alternate SEs for other source or destination can be obtained. Figure 4.2 shows the redundancy graph of IAON. In this graph, the source and destination are shown by empty circle. In figure 4.2, all the SEs are depicted by black nodes. Redundancy graph tells that the IAON has the potency of good communication in faulty and non-faulty situations.

![Figure 4.2 Redundancy Graph of IAON](image)

### 4.3.2 Routing Algorithm of IAON

The routing algorithm of IAON shows that how the data packets can be routed through the network in non-faulty, single switch faulty, and double switch faulty conditions. As an input, initially the user will enter the size of network (N) and as an output he will get the status that the transmitted data packets reached on N destinations or not reached. The routing algorithm of IAON is shown in figure 4.3
Algorithm_IAON_Broadcast
Input: N
Output: Data Packets Successfully Reached on N Destinations or Network Fails

BEGIN
1. for i = 0 to N
2. Source = i
3. FIRST-STAGE (Source)

FIRST-STAGE (Source)
1. if SE\(p_1\) == F
2. First_Altarate_SE\(1\)
3. else SECOND-STAGE (Source)
4. if First_Altarate_SE\(1\) == F
5. Second_Altarate_SE\(1\)
6. else SECOND-STAGE (Source)
7. if Second_Altarate_SE\(1\) == F
8. Network Fails
9. else SECOND-STAGE (Source)

SECOND-STAGE (Source)
1. if SE-e == F
2. SE-f
3. else THIRD-STAGE (Source)
4. if SE-f == F
5. SE-g
6. else THIRD-STAGE (Source)
7. if SE-g == F
8. Network Fails
9. else THIRD-STAGE (Source)

THIRD-STAGE (Source)
1. if SE\(p_3\) == F
2. First_Altarate_SE\(3\)
3. else Collect data packets on SE\(p_3\) and Send to N destinations
4. if First_Altarate_SE\(3\) == F
5. Second_Altarate_SE\(3\)
6. else Collect data packets on First_Altarate_SE\(3\) and Send to N destinations
7. if Second_Altarate_SE\(3\) == F
8. Network Fails
9. else Collect data packets on Second_Altarate_SE\(3\) and Send to N destinations

END

Figure 4.3. Routing Algorithm of IAON.
This network has 3 functions which are as follows:

- FIRST-STAGE (Source)
- SECOND-STAGE (Source)
• THIRD-STAGE (Source)

The main functionality of all these functions is to provide a suitable path in such a way that in faulty or non-faulty conditions data packets can be reached from a given source to all N destinations. If it is found that 1 SE or 2 SEs of a stage are faulty then data packets will arrive on another SE of that particular stage. The SE which collects the data packets will send them towards the N destinations. This is the complete routing process of IAON.

4.3.2.1 Proof of Correctness

To prove the algorithm the author has taken an example which is as follows:

Example 1: It is assumed that the source is 5 and data packets have to be sent to N destinations. In this example, the author has considered three cases which are as follows:

Case 1: When SEs are not faulty in every stage.

If the network is non-faulty then the primary routes of source 5 will be as follows:

Route 1: b-e-h,
Route 2: b-e-i,
Route 3: b-e-j,
Route 4: b-e-k.

After reaching on SE-h, SE-i, SE-j and SE-k data packets will be transmitted to all the given destinations through Demux. The routes are shown by dotted lines in figure 4.4.
Case 2: When 1 SE of each stage is faulty

Here it is assumed that SEs b, e and h are faulty. In this case the first alternate routes of source 5 will be as follows:

Route 1: a-f-i,
Route 2: a-f-j,
Route 3: a-f-k.

In figure 4.5, it can be seen that SE-b has connectivity with SE-a through Mux. Therefore, SE-a will be the first alternate SE of stage 1 for source 5. In the same way, SE-f will be the first alternate SE of stage 2 for source 5. In figure 4.5, it can be seen that SE-h has connectivity with SE-j and SE-j. Hence, SE-i and SE-j will become the first alternate SEs of stage 2. The routes are shown by dotted lines in figure 4.5.
Case 3: When 2 SEs of each stage are faulty.

Here it is assumed that SEs b, a, e, f, h and i are faulty. In this case the second alternate routes of source 5 will be as follows:

Route 1: $d-g-j$,
Route 2: $d-g-k$.

In figure 4.6, it can be seen that SE-b has connectivity with SE-d through a Mux. Therefore, SE-d will be the second alternate SE of stage 1 for source 5. In the same way, SE-g will be the second alternate SE of stage 2 for source 5. In figure 4.6, it can be seen that SE-h and SE-i have connected with SE-j and SE-k. Hence, SE-j and SE-k will become the second alternate SEs of stage 2. The routes are shown by dotted lines in figure 4.6.
Here the author has discussed three cases. This discussion shows that the proposed MIN is a double fault tolerant interconnection network means it can sustain 2 faulty SEs in each stage simultaneously. If the network has more than 2 faulty SE in each stage simultaneously, then the network will fail in order to provide the alternate routes.

Theorem: There are at least 21 routes between every source and destination address.

Proof: In the previous subsections, it is shown in all figures of IAON that the second stage of IAON unites the SEs of first stage and third stage. It means that the second stage is a very important stage of IAON. The other point is that all the alternate routes are generated because of second stage. In IAON, when data packets come from any SE of first stage via any source, then definitely they will go on any one SE of second stage. In this case, the routes via SEs of the second stage will be as follows:
Route 1: SE1-e-SE3,
Route 2: SE1-f-SE3,
Route 3: SE1-g-SE3,
Route 4: SE1-e-f-SE3,
Route 5: SE1-f-e-SE3,
Route 6: SE1-f-g-SE3,
Route 7: SE1-g-f-SE3.

Furthermore, it is already discussed that every source is allied with 3 SEs of stage 1. Therefore, total available routes will be

$\text{IAON}_{\text{Route}} = (7 \times \text{Allied SE1}),$
$\text{IAON}_{\text{Route}} = (7 \times 3),$
$\text{IAON}_{\text{Route}} = 21.$

$\text{IAON}_{\text{Route}}$ represents the total number of routes in IAON. Therefore, it is proved that the network has at least 21 routes between every source and destination. To understand the theorem appropriately the author has taken an example.

Example 2: It is assumed that the source is 9 and the destination is 2. In figure 4.1, it can be observed that source 9 has connectivity with SEs c, a and d. Further, a destination 2 has connectivity with SEs h, i and j. Therefore, the possible alternate routes will be as follows:

Route 1: c-e-h,
Route 2: c-f-h,
Route 3: c-g-h,
Route 4: c-e-f-h,
Route 5: c-f-e-h,
Route 6: c-f-g-h,
Route 7: c-g-f-h,
Route 8: a-e-h,
Route 9: a-f-h,
Route 10: a-g-h,
Route 11: a-e-f-h,
Route 12: a-f-e-h,
Route 13: a-f-g-h,
Route 14: a-g-f-h,
Route 15: d-e-h,
Route 16: d-f-h,
Route 17: d-g-h,
Route 18: d-e-f-h,
Route 19: d-f-e-h,
Route 20: d-f-g-h,
Route 21: d-g-f-h.

Therefore, again, it is proved that there are at least 21 routes between every source and destination address.

4.4 Irregular Augmented Shuffle Exchange Network-3
This section gives a detailed description of IAON.

4.4.1 Structure of Irregular Augmented Shuffle Exchange Network-3
The structure of irregular augmented shuffle exchange network-3 is based on IASEN-2. In figure 4.7, it can be seen that it has 16 sources and 16 destinations, hence the size of IASEN-3 is $N = 16$. 
In figure 4.7, the source address, destination address, multiplexer and demultiplexer are represented by S, D, Mux and Demux respectively. This is a 3-stage MIN. In first and last stage, each source or each destination is connected with three SEs of that particular stage, e.g. source 11 is connected with SE $f$, $a$ and $d$ and therefore $f$, $a$ and $d$ are the primary, first alternate and second alternate SEs for source 11. In the same way, the primary, first alternate and second alternate SEs for another source and destinations can be obtained. The size of each SE in first and third stage is $2 \times 3$ and $3 \times 2$ respectively. In stage 2, the size of each SE is $8 \times 8$.

4.4.2 Routing Algorithm of IASEN-3

The routing algorithm of IASEN-3 is given in figure 4.8.
Algorithm IASEN-3
Input: N, Source, Destinations
Output: Data Packets Reached Successfully or Network Fails
BEGIN
1. if PSE1 == F || PSE3 == F
2. then AE1
3. else Send data packets to Next Appropriate Node
4. if AE1 == F
5. then AF?
6. else Send data packets to Next Appropriate Node
7. if AE2 == F
8. then Network Fails
9. if SE-i == F
10. then SE-j
11. else Send data packets to Appropriate SE of Third Stage
12. if SE-j == F
13. then Network Fails
14. else Send data packets to Appropriate SE of Third Stage
End

Figure 4.8 Routing algorithm of IASEN-3.

In the routing algorithm of IASEN-3, if data packets arrive at the primary SE of the first stage (PSE1) or primary SE of third stage (PSE3), then that particular SE will be checked that whether it is faulty or non-faulty. If it is noticed that the required SE is faulty then the first alternate SE (AE1) of the first stage will get the data packets. If AE1 is also faulty then second alternate SE (AE2) of the first stage will get the data packets. In case all the SEs i.e. PSE1, AE1 and AE2 of first stage or PSE3, AE1 and AE2 of third stage are not responding properly then the network will fail. If data packets arrive at SE i of second stage and it is faulty then SE j of the second stage will receive the request. If it is noticed that all the required SEs of a stage are faulty then the network will fail. Finally, it can be said that, if the required SEs of all three stages are in working condition, then data will be transmitted from the given source to its given destinations otherwise the data transmis-
sion process will be stopped. In the third step of the algorithm the term “Node” may be the SE of second stage or the given destination.

Theorem: IASEN-3 shows single switch fault tolerability in each stage simultaneously.

Proof: To prove the theorem the author has taken an example which is as follows:

Example 3: It is assumed that the source is 2 and the destination is 9 and SEs b, i, and o are faulty. In this situation the rest of the routes are as follows:

Route 1: 2-6-Mux-d-j-k-Demux-1-9
Route 2: 2-10-Mux-f-j-k-Demux-1-9
Route 3: 2-6-Mux-d-j-q-Demux-13-9
Route 4: 2-10-Mux-f-j-q-Demux-13-9

These available paths prove that IASEN-3 is a single switch fault tolerant network in every stage.

4.5 Performance Analysis and Simulation Results

In this section, the author has presented all the results which he has got in the simulations. The performance of MALN [21], IASEN-2 and IAON are obtained in non-faulty and single switch faulty conditions. It is observed that IAON has better performance than the MALN and IASEN-2 in both conditions. The reasons are as follows:

i) IAON has better bandwidth than the MALN and IASEN-2.

ii) If a network has good bandwidth means it will have good throughput, good processor utilization and good processing power. Therefore IAON is better than the MALN and IASEN-2.

iii) It has better probability of acceptance (PA) than the MALN and IASEN 2. PA of IAON is better means the packet loss probability in IAON is less than the MALN and IASEN-2.

iv) Further, IAON is double switch fault tolerant MIN means it can sustain 2 faulty SEs in stage simultaneously whereas MALN and IASEN-2 are single switch fault tolerant MIN means these MINs can sustain single faulty SE in each stage simultaneously.
Further, the author has compared the performance of IASEN-2, IAON and IASEN-3 in non-faulty and single switch faulty conditions. It is observed that IASEN-3 has better performance than the IASEN-2 and IAON in both conditions. IASEN-3 has the same reasons of better performance as the IAON has, except the last (4th) reason. IASEN-3 is a single switch fault tolerant network. The author has also shown the performance of IAON in non-faulty, single switch faulty and double switch faulty conditions. The author has considered the bandwidth, the probability of acceptance, transmission time, throughput, processor utilization, and processing power as the factors of performance. The descriptions of all these factors are given in the next subsections.

4.5.1 Load Factor

The term load factor or request generation probability means that how much load is offered to the network for the data transmission. Here, the load factor has 10 different values start from 0.1 and goes up to 1 by adding 0.1 in the previous value [16, 21, 22]. Different numbers of data packets are transmitted from the given source to all destinations on each value of load factor. In this simulation the author has considered the following table:

<table>
<thead>
<tr>
<th>Load Factor (p)</th>
<th>Total Number of Data packets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>50</td>
</tr>
<tr>
<td>0.2</td>
<td>100</td>
</tr>
<tr>
<td>0.3</td>
<td>150</td>
</tr>
<tr>
<td>0.4</td>
<td>200</td>
</tr>
<tr>
<td>0.5</td>
<td>250</td>
</tr>
<tr>
<td>0.6</td>
<td>300</td>
</tr>
<tr>
<td>0.7</td>
<td>350</td>
</tr>
<tr>
<td>0.8</td>
<td>400</td>
</tr>
<tr>
<td>0.9</td>
<td>450</td>
</tr>
<tr>
<td>1.0</td>
<td>500</td>
</tr>
</tbody>
</table>

Table 4.3. Load on Given Load Factors.
According to table 4.3, the author has transmitted the data packets through MALN, IASEN-2, IAON, and IASEN-3 in faulty and non-faulty conditions on each value of load factor. Here the term "faulty" means single switch fault for MALN, IASEN-2, and IASEN-3. For IAON, "faulty" means single and double switch faulty conditions. The size of each data packet is 1 byte in the simulation.

4.5.2 Calculation of Bandwidth
To calculate the bandwidth (BW), the author has applied the probabilistic method on MALN [21], IASEN-2, IAON and IASEN-3. To understand the probabilistic method, he has given an example. It is assumed that a SE k has x number of input lines and y number of output lines and therefore the size of the SE is x×y. When data packets arrive on SE k then it collects them and forward to other SE or destination. Hence, according to probabilistic method [16]:

- If the data packets are not arriving on SE k then the probability will be \(1 - (p/y)\). Here p is the load factor or probability of data packets which are generated by a source.
- If the data packets are not arriving on SE k from "x" input lines, then the probability will be \((1 - (p/y))^x\).
- If the data packets are arriving on one output line of SE k from "x" input lines of SE k then the probability will be \(1 - (1 - (p/y))^x\).

Therefore, SE k passes the total number of data packets per unit time will be \(y - (1 - (p/y))^x\). A MIN consists of more than one stage and each stage has a certain number of SEs. Hence, the output rate of a stage will become the input rate of the next stage. Based on this phenomenon the author has calculated the BW of MALN, IASEN-2, IAON, and IASEN-3. Basically, bandwidth is the capacity of a network. It can be defined as follows:

Definition 1: "Bandwidth is the maximum rate at which information can be transferred [5, 16, 21, 22]."
Based on the probabilistic method, BWof a MIN will be \( = (\text{total number of output lines } \times p) \text{ bytes/second} \).

Hence, probability equations of MALN [21]:

\[
\begin{align*}
    p_1 &= 1-(1-\frac{p_0}{3})^3 \\
    p_2 &= 1-(1-\frac{p_1}{6})^3 \\
    p_3 &= 1-(1-\frac{p_2}{3})^3 \\
    p_4 &= 1-\{(1-p_3) \times \left(1-\frac{p_1}{2}\right)^2\} \\
    BW_{MALN} &= (N \times p_4)
\end{align*}
\]

Here \( p_1 \), \( p_2 \), \( p_3 \) and \( p_4 \) represents the load (data packets) arrived on the SEs of first, second, third, and fourth stage of MALN.

Probability equations of IASEN-2:

\[
\begin{align*}
    p_1 &= 1-(1-\frac{p_0}{3})^2 \\
    p_2 &= 1-(1-\frac{p_1}{6})^9 \\
    p_3 &= 1-(1-\frac{p_2}{9})^3 \\
    p_4 &= 1-\{(1-p_3) \times \left(1-\frac{p_1}{2}\right)^3\} \\
    BW_{IASEN-2} &= (N \times p_4)
\end{align*}
\]

Here \( p_1 \), \( p_2 \), \( p_3 \) and \( p_4 \) represents the load (data packets) arrived on the SEs of first, second, third and fourth stage of IASEN 2.

Probability equations of IAON:

\[
\begin{align*}
    p_1 &= 1-(1-\frac{p_0}{4})^4 \\
    p_2 &= 1-(1-\frac{p_1}{16})^5 \\
    p_3 &= 1-\{(1-p_2) \times \left(1-\frac{p_1}{4}\right)^4\} \\
    BW_{IAON} &= (N \times p_3)
\end{align*}
\]

Here \( p_1 \), \( p_2 \), and \( p_3 \) represents the load (data packets) arrived on the SEs of first, second and third stage of IAON.
Probability equations of IASEN-3:

\[ p_1 = 1 - (1 - \frac{p_0}{3})^2 \]
\[ p_2 = 1 - (1 - \frac{p_1}{8})^8 \]
\[ p_3 = 1 - [(1 - p_2) \times \left(1 - \frac{p_1}{2}\right)]^3 \]
\[ RW_{IASEN-3} = (N \times p_3) \]

Here \( p_1, p_2, \) and \( p_3 \) represents the load (data packets) arrived on the SEs of first, second and third stage of IASEN-3.

### 4.5.3 Calculation of Probability of Acceptance

It is not certain that the total number of data packets which are transmitted from a source and the total number of data packets which are accepted by \( N \) destinations will be the same. Loss of data packets occurs during the data transmission process because of switch failure, link failure, or any other reason. Therefore, the probability of acceptance (PA) gives the information that how many data packets will be accepted by \( N \) destinations. It can be defined as follows [5, 21]:

*Definition 2: “Probability of Acceptance is defined as the ratio of the expected bandwidth to the expected number of requests generated per cycle [5, 21, 22].”*

Therefore, PA of MALN, IASEN-2, IAON and IASEN-3 will be as follows:

\[ PA_{MALN} = \left(\frac{BW_{MALN}}{N \times p}\right) \]
\[ PA_{IASEN-2} = \left(\frac{BW_{IASEN-2}}{N \times p}\right) \]
\[ PA_{IAON} = \left(\frac{BW_{IAON}}{N \times p}\right) \]
\[ PA_{IASEN-3} = \left(\frac{BW_{IASEN-3}}{N \times p}\right) \]

### 4.5.4 Calculation of Transmission Time

The transmission time is the time which is taken by the data packets from any source to any given destination [1-6]. To calculate the transmission time the author has taken some assumptions.
To understand the transmission time, the author has taken a sample network, which is shown in figure 4.9.

![Sample Network](image)

Figure 4.9. Sample Network.

In figure 4.9, source and destination node is shown by dotted circle and a solid circle respectively. It has three stages therefore; a data packet can take any one route:

Route1: Source - SE1 - SE3 - SE5 - Destination,
Route2: Source - SE1 - SE4 - SE5 - Destination,
Route3: Source - SE1 - SE3 - SE6 - Destination,
Route4: Source - SE1 - SE4 - SE6 - Destination,
Route5: Source - SE2 - SE3 - SE5 - Destination,
Route6: Source - SE2 - SE4 - SE5 - Destination,
Route7: Source - SE2 - SE3 - SE6 - Destination,
Route8: Source - SE2 - SE4 - SE6 - Destination.

It is assumed that a data packet takes 1 second from one node to another node in non-faulty condition. Here the nodes may be any SE or any processor. Therefore, the transmission time of a data packet will be 4 seconds. It means if the number of stages is 3 then transmission time of a data packet is $3+1=4$ seconds.

Hence, if the number of stages in a MIN is $q$ then transmission time of a data packet will be:

$$TT_1 = (q + 1)$$

Here $TT_1$ is the transmission time of a single data packet. If there are $i$ numbers of data packets which are to be sent from a given source to $N$ destinations then transmission time will be:
\[ TT_i = (q + i) \]

Here \( TT_i \) is the transmission time of \( i \) number of data packets. Calculation of \( TT_i \) can be understood by figure 4.9.

![Figure 4.10. Calculation of Data Transmission Time.](image)

In figure 4.10, when a data packet will move from the SE1 to the SE2 of the next stage, then in the mean time the second data packet will take the route from source to SE1. Therefore, if the size of the network is 16, then transmission time will be as follows:

\[ TT_{16} = (q + i) \]

\( TT_{16} \) is the transmission time of a network of size 16.

- If the size of the network (N) will increase then the number of SEs in each stage will also increase. Therefore, the \( TT_i \) will increase. In this chapter, the minimum network size is \( N=16 \) for each network. The transmission time for a large network will be calculated as follows:

\[ TT_{N} = (TT_{16} + \left( \frac{N}{16} - 1 \right)) \]

Here, \( TT_{N} \) is the transmission time of a network of size \( N \).

- If the network is faulty then data packets will take extra transmission time. It is assumed that if \( k \) SEs are faulty then extra \( k \) seconds will be taken by the data packets. In this case, the total transmission time will be as follows:

\[ TT_{\text{faulty}} = TT_{N} + k \]

Here, \( TT_{\text{faulty}} \) is the transmission time of a network in faulty condition.

Therefore, the transmission time of MALN, IASEN-2, IAON and IASEN-3 in non-faulty case will be as follows:

\[ TT_{N,\text{MALN}} = (TT_{16,\text{MALN}} + \left( \frac{N}{16} - 1 \right)) \]

\[ TT_{N,\text{IASEN-2}} = (TT_{16,\text{IASEN-2}} + \left( \frac{N}{16} - 1 \right)) \]
\[ \text{TT}_{i,N,IAON} = \left\{ \text{TT}_{i,16,IAON} + \left( \frac{N}{16} - 1 \right) \right\} \]

\[ \text{TT}_{i,N,IASEN-3} = \left\{ \text{TT}_{i,16,IASEN-3} + \left( \frac{N}{16} - 1 \right) \right\} \]

Therefore, the transmission time of MALN, IASEN-2, IAON and IASEN-3 in the faulty case will be as follows:

\[ \text{TT}_{\text{faulty,MALN}} = (\text{TT}_{i,N,\text{MALN}} + k) \]

\[ \text{TT}_{\text{faulty,IASEN-2}} = (\text{TT}_{i,N,\text{IASEN-2}} + k) \]

\[ \text{TT}_{\text{faulty,IAON}} = (\text{TT}_{i,N,\text{IAON}} + k) \]

\[ \text{TT}_{\text{faulty,IASEN-3}} = (\text{TT}_{i,N,\text{IASEN-3}} + k) \]

In this way the author has calculated the transmission time of data packets which are transmitted through the MALN, IASEN-2, IAON and IASEN-3.

4.5.5 Calculation of Throughput

In a network, throughput (TP) means the average number of data packets accepted by the given network. It depends on the bandwidth and transmission time of the network. It can be defined as follows [5, 21, 22]:

*Definition 3: “Throughput means the average number of cells delivered by a network per unit time [1-6, 21,22].”*

Therefore, the TP of MALN, IASEN-2, IAON and IASEN-3 in non-faulty conditions are as follows [5, 21, 22]:

\[ \text{TP}_{\text{MALN}} = \left( \frac{\text{BW}_{\text{MALN}}}{N \times \text{TT}_{i,N,\text{MALN}}} \right) \]

\[ \text{TP}_{\text{IASEN-2}} = \left( \frac{\text{BW}_{\text{IASEN-2}}}{N \times \text{TT}_{i,N,\text{IASEN-2}}} \right) \]

\[ \text{TP}_{\text{IAON}} = \left( \frac{\text{BW}_{\text{IAON}}}{N \times \text{TT}_{i,N,\text{IAON}}} \right) \]

\[ \text{TP}_{\text{IASEN-3}} = \left( \frac{\text{BW}_{\text{IASEN-3}}}{N \times \text{TT}_{i,N,\text{IASEN-3}}} \right) \]

The TP of MALN, IASEN-2, IAON and IASEN-3 in faulty conditions are as follows:

\[ \text{TP}_{\text{faulty,MALN}} = \left( \frac{\text{BW}_{\text{MALN}}}{N \times \text{TT}_{\text{faulty,MALN}}} \right) \]
\[ TP_{\text{faulty, IASEN-2}} = \left( \frac{BW_{\text{IASEN-2}}}{N \times TT_{\text{faulty, IASEN-2}}} \right) \]

\[ TP_{\text{faulty IAON}} = \left( \frac{BW_{\text{IAON}}}{N \times TT_{\text{faulty, IAON}}} \right) \]

\[ TP_{\text{faulty, IASEN-3}} = \left( \frac{BW_{\text{IASEN-3}}}{N \times TT_{\text{faulty, IASEN-3}}} \right) \]

In this way the author has calculated the throughput of MALN, IASEN-2, IAON and IASEN-3.

4.5.6 Calculation of Processor Utilization

Processor utilization (PU) means the time consumed by the processor in order to process the given workload. It depends on the given workload, the bandwidth of the network, and transmission time. Here the term “workload” refers the load factor. It can be defined as follows [1-6, 21, 22]:

Definition 4: “Processor Utilization is the expected percentage of time; a processor is active doing internal computation without accessing the global memory [5, 21, 22].”

Therefore, the PU of MALN, IASEN-2, IAON and IASEN-3 in non-faulty conditions are as follows [5, 21, 22]:

\[ PU_{\text{MALN}} = \left( \frac{TP_{\text{MALN}}}{p} \right) \]

\[ PU_{\text{IASEN-2}} = \left( \frac{TP_{\text{IASEN-2}}}{p} \right) \]

\[ PU_{\text{IAON}} = \left( \frac{TP_{\text{IAON}}}{p} \right) \]

\[ PU_{\text{IASEN-3}} = \left( \frac{TP_{\text{IASEN-3}}}{p} \right) \]

The PU of MALN, IASEN-2, IAON and IASEN-3 in faulty conditions are as follows:

\[ PU_{\text{faulty, MALN}} = \left( \frac{TP_{\text{faulty, MALN}}}{p} \right) \]

\[ PU_{\text{faulty, IASEN-2}} = \left( \frac{TP_{\text{faulty, IASEN-2}}}{p} \right) \]
\[ PU_{\text{faulty IAON}} = \left( \frac{TP_{\text{faulty IAON}}}{p} \right) \]
\[ PU_{\text{faulty IASEN-3}} = \left( \frac{TP_{\text{faulty IASEN-3}}}{p} \right) \]

In this way the author has calculated the processor utilization of MALN, IASEN-2, IAON, and IASEN-3.

4.5.7 Calculation of Processing Power

The calculation of processing power (PP) is based on the processors which are used in order to complete the given workload. It depends on the processor utilization. It can be defined as follows [5, 21, 22]:

*Definition 5*: “Processing Power is defined as the sum of processor utilization over the number of processors [5, 21, 22].”

Therefore, the PP of MALN, IASEN-2, IAON and IASEN-3 in non-faulty conditions are as follows [5, 21, 22]:
\[ PP_{\text{MALN}} = (PU_{\text{MALN}} \times N) \]
\[ PP_{\text{IASEN-2}} = (PU_{\text{IASEN-2}} \times N) \]
\[ PP_{\text{IAON}} = (PU_{\text{IAON}} \times N) \]
\[ PP_{\text{IASEN-3}} = (PU_{\text{IASEN-3}} \times N) \]

Therefore, the PP of MALN, IASEN-2, IAON and IASEN-3 in faulty conditions are as follows:
\[ PP_{\text{faulty MALN}} = (PU_{\text{faulty MALN}} \times N) \]
\[ PP_{\text{faulty IASEN-2}} = (PU_{\text{faulty IASEN-2}} \times N) \]
\[ PP_{\text{faulty IAON}} = (PU_{\text{faulty IAON}} \times N) \]
\[ PP_{\text{faulty IASEN-3}} = (PU_{\text{faulty IASEN-3}} \times N) \]

In this way the author has calculated the processing power of MALN, IASEN-2, IAON and IASEN-3.

Note: In this chapter the author has taken the assumption that when the size of the network will increase then the number of SEs in each stage will increase. In his published work, he has taken the assumption that when the size of the network will increase then the size of SEs will increase.
4.5.8 Bandwidth for MALN, IASEN-2 and IAON

In figure 4.11, 4.12, 4.13 and 4.14, the author has shown the bandwidth of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. In all figures, it is clear that the IAON has better bandwidth than the earlier proposed MINs.

Figure 4.11. Comparison of BW for MALN, IASEN-2 and IAON when N=16.

Figure 4.12. Comparison of BW for MALN, IASEN-2 and IAON when N=32.
4.5.9 Probability of Acceptance for MALN, IASEN-2 and IAON

In figure 4.15, the author has shown the bandwidth of MALN, IASEN-2 and IAON. In this figure, it is clear that the IAON has a better probability of acceptance than the earlier proposed MINs.
4.5.10 Throughput for MALN, IASEN-2 and IAON in Non-Faulty Condition

In figure 4.16, 4.17, 4.18 and 4.19, the author has shown the throughput of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. In all figures, it is clear that the IAON has better throughput than the earlier proposed MINs. Here the throughput is calculated in non-faulty condition.

Figure 4.16. Comparison of TP for MALN, IASEN-2 and IAON when N=16 in Non-Faulty Condition.
Figure 4.17. Comparison of TP for MALN, IASEN-2 and IAON when N=32 in Non-Faulty Condition.

Figure 4.18. Comparison of TP for MALN, IASEN-2 and IAON when N=64 in Non-Faulty Condition.

Figure 4.19. Comparison of TP for MALN, IASEN-2 and IAON when N=128 in Non-Faulty Condition.
4.5.11 Throughput for MALN, IASEN-2 and IAON in Single Switch Faulty Condition

In figure 4.20, 4.21, 4.22 and 4.23, the author has shown the throughput of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. Here the throughput is calculated in single switch faulty condition. In all figures, it is clear that the IAON has better throughput than the earlier proposed MINs.

Figure 4.20. Comparison of TP for MALN, IASEN-2 and IAON when N=16 in Single Switch Faulty Condition.

Figure 4.21. Comparison of TP for MALN, IASEN-2 and IAON when N=32 in Single Switch Faulty Condition.
Figure 4.22. Comparison of TP for MALN, IASEN-2 and IAON when N=64 in Single Switch Faulty Condition.

Figure 4.23. Comparison of TP for MALN, IASEN-2 and IAON when N=128 in Single Switch Faulty Condition.

4.5.12 Processor Utilization for MALN, IASEN-2 and IAON in Non-Faulty Condition

In figure 4.24, 4.25, 4.26 and 4.27, the author has shown the processor utilization of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in non-faulty condition. In all figures, it is clear that the IAON has better processor utilization than the earlier proposed MINs.
Figure 4.24. Comparison of PU for MALN, IASEN-2 and IAON when N=16 in Non-Faulty Condition.

Figure 4.25. Comparison of PU for MALN, IASEN-2 and IAON when N=32 in Non-Faulty Condition.

Figure 4.26. Comparison of PU for MALN, IASEN-2 and IAON when N=64 in Non-Faulty Condition.
4.5.13 Processor Utilization for MALN, IASEN-2 and IAON in Single Switch Faulty Condition

In figure 4.28, 4.29, 4.30 and 4.31, the author has shown the processor utilization of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in single switch faulty condition. In all figures, it is clear that the IAON has better processor utilization than the earlier proposed MINS.
Figure 4.29. Comparison of PU for MALN, IASEN-2 and IAON when N=32 in Single Switch Faulty Condition.

Figure 4.30. Comparison of PU for MALN, IASEN-2 and IAON when N=64 in Single Switch Faulty Condition.

Figure 4.31. Comparison of PU for MALN, IASEN-2 and IAON when N=128 in Single Switch Faulty Condition.
4.5.14 Processing Power for MALN, IASEN-2 and IAON in Non-Faulty Condition

In figure 4.32, 4.33, 4.34 and 4.35, the author has shown the processing power of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in non-faulty condition. In all figures, it is clear that the IAON has better processing power than the earlier proposed MINs.

![Figure 4.32. Comparison of PP for MALN, IASEN-2 and IAON when N=16 in Non-Faulty Condition.](image1)

![Figure 4.33. Comparison of PP for MALN, IASEN-2 and IAON when N=32 in Non-Faulty Condition.](image2)

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4.5.15 Processing Power for MALN, IASEN-2 and IAON in Single Switch Faulty Condition

In figure 4.36, 4.37, 4.38 and 4.39, the author has shown the processing power of MALN, IASEN-2 and IAON for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in single switch faulty condition.
In all figures, it is clear that the IAON has better processing power than the earlier proposed MINs.

Figure 4.36. Comparison of PP for MALN, IASEN-2 and IAON when N=16 in Single Switch Faulty Condition.

Figure 4.37. Comparison of PP for MALN, IASEN-2 and IAON when N=32 in Single Switch Faulty Condition.
Figure 4.38. Comparison of PP for MALN, IASEN-2 and IAON when N=64 in Single Switch Faulty Condition.

Figure 4.39. Comparison of PP for MALN, IASEN-2 and IAON when N=128 in Single Switch Faulty Condition.

Here the author has shown the simulation results of MALN, IASEN-2 and IAON (from figure 4.11 to 4.39). Further he calculated the average PA which is as follows:
<table>
<thead>
<tr>
<th>Network</th>
<th>PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>MALN</td>
<td>0.561</td>
</tr>
<tr>
<td>IASEN-2</td>
<td>0.564</td>
</tr>
<tr>
<td>IAON</td>
<td>0.588</td>
</tr>
</tbody>
</table>

**Table 4.4**

The table 4.4 clearly shows that the PA of MALN and IASEN-2 are 56.1% and 56.4% whereas PA of IAON is 58.8%. It means IAON is 2.7% better than MALN and 2.4% better than IASEN-2 in terms of PA. Further, it is observed that performance of a network is primarily depending on the bandwidth because most of the factors of performance (e.g. TP, PU, PP) are calculated on the basis of bandwidth. Therefore, the author has calculated the average bandwidth which is follows:

<table>
<thead>
<tr>
<th>N</th>
<th>MALN</th>
<th>IASEN-2</th>
<th>IAON</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>8.983</td>
<td>9.032</td>
<td>9.420</td>
</tr>
<tr>
<td>32</td>
<td>17.966</td>
<td>18.065</td>
<td>18.840</td>
</tr>
<tr>
<td>64</td>
<td>35.933</td>
<td>36.130</td>
<td>37.680</td>
</tr>
<tr>
<td>128</td>
<td>71.866</td>
<td>72.261</td>
<td>75.360</td>
</tr>
</tbody>
</table>

**Table 4.5**

From table 4.5, it is observed that when size of network is doubled then value of bandwidth also gets doubled. So,

For MALN->

\[
\left( \frac{8.983}{16} \right) \times 100 = 56.1\%
\]

Here the size of network is 16 hence the author has taken the value 16 in denominator and multiplied by 100 to calculate the percentage.

For IASEN-2=>

\[
\left( \frac{9.032}{16} \right) \times 100 = 56.4\%
\]

For IAON=>

\[
\left( \frac{9.420}{16} \right) \times 100 = 58.8\%
\]
Again, it is observed that IAON is 2.7% better than MALN and 2.4% better than IASEN-2.

4.5.16 Bandwidth for IASEN-2, IAON and IASEN-3

In figure 4.40, 4.41, 4.42 and 4.43, the author has shown the bandwidth of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. In all figures, it is clear that the IASEN-3 has better bandwidth than the IASEN-2 and IAON.

![BW When N=16](image)

Figure 4.40. Comparison of BW for IASEN-2, IAON and IASEN-3 when N=16.
Figure 4.41. Comparison of BW for IASEN-2, IAON and IASEN-3 when N=32.

Figure 4.42. Comparison of BW for IASEN-2, IAON and IASEN-3 when N=64.

Figure 4.43. Comparison of BW for IASEN-2, IAON and IASEN-3 when N=128.
4.5.17 Probability of Acceptance for IASEN-2, IAON and IASEN-3

In figure 4.44, the author has shown the bandwidth of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. In all figures, it is clear that the IASEN-3 has a better probability of acceptance than the IASEN-2 and IAON.

![Graph of PA of IASEN2, IAON and IASEN3](image)

*Figure 4.44 Comparison of PA for IASEN-2, IAON and IASEN-3*

4.5.18 Throughput for IASEN-2, IAON and IASEN-3 in Non-Faulty Condition

In figure 4.45, 4.46, 4.47 and 4.48, the author has shown the throughput of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. Here the throughput is calculated in non-faulty condition. In all figures, it is clear that the IASEN-3 has better throughput than the IASEN-2 and IAON.
Figure 4.45. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=16 in Non-Faulty Condition.

Figure 4.46. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=32 in Non-Faulty Condition.

Figure 4.47. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=64 in Non-Faulty Condition.
4.5.19 Throughput for IASEN-2, IAON and IASEN-3 in Single Switch Faulty Condition

In figure 4.49, 4.50, 4.51 and 4.52, the author has shown the throughput of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. Here the throughput is calculated in single switch faulty condition. In all figures, it is clear that the IASEN-3 has better throughput than the IASEN-2 and IAON.

Figure 4.48. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=128 in Non-Faulty Condition.

Figure 4.49. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=16 in Single Switch Faulty Condition.
Figure 4.50. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=32 in Single Switch Faulty Condition.

Figure 4.51. Comparison of TP for IASEN-2, IAON and IASEN-3 when N=64 in Single Switch Faulty Condition.
4.5.20 Processor Utilization for IASEN-2, IAON and IASEN-3 in Non-Faulty Condition

In figure 4.53, 4.54, 4.55 and 4.56, the author has shown the processor utilization of IASEN-2, IAON and IASEN-3 for $N=16$, 32, 64 and 128 respectively. Here the processor utilization is calculated in non-faulty condition. In all figures, it is clear that the IASEN-3 has better processor utilization than the IASEN-2 and IAON.
Figure 4.54. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=32 in Non-Faulty Condition.

Figure 4.55. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=64 in Non-Faulty Condition.
4.5.21 Processor Utilization for IASEN-2, IAON and IASEN-3 in Single Switch Faulty Condition

In figure 4.57, 4.58, 4.59 and 4.60, the author has shown the processor utilization of IASEN-2, IAON and IASEN-3 for $N=16$, 32, 64 and 128 respectively. Here the processor utilization is calculated in single switch faulty condition. In all figures, it is clear that the IASEN-3 has better processor utilization than the IASEN-2 and IAON.

Figure 4.56. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=128 in Non-Faulty Condition.

Figure 4.57. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=16 in Single Switch Faulty Condition.
Figure 4.58. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=32 in Single Switch Faulty Condition.

Figure 4.59. Comparison of PU for IASEN-2, IAON and IASEN-3 when N=64 in Single Switch Faulty Condition.
4.5.22 Processing Power for IASEN-2, IAON and IASEN-3 in Non-Faulty Condition

In figure 4.61, 4.62, 4.63 and 4.64, the author has shown the processor utilization of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in non-faulty condition. In all figures, it is clear that the IASEN-3 has better processor utilization than the IASEN-2 and IAON.
Figure 4.62. Comparison of PP for IASEN-2, IAON, and IASEN-3 when N=32 in Non-Faulty Condition.

Figure 4.63. Comparison of PP for IASEN-2, IAON, and IASEN-3 when N=64 in Non-Faulty Condition.
Figure 4.64. Comparison of PP for IASEN-2, IAON and IASEN-3 when N=128 in Non-Faulty Condition.

4.5.23 Processing Power for IASEN-2, IAON and IASEN-3 in Single Switch Faulty Condition

In figure 4.65, 4.66, 4.67 and 4.68, the author has shown the processor utilization of IASEN-2, IAON and IASEN-3 for N=16, 32, 64 and 128 respectively. Here the processor utilization is calculated in single switch faulty condition. In all figures, it is clear that the IASEN-3 has better processor utilization than the IASEN-2 and IAON.

Figure 4.65. Comparison of PP for IASEN-2, IAON and IASEN-3 when N=16 in Single Switch Faulty Condition.
Figure 4.66. Comparison of PP for IASEN-2, IAON and IASEN-3 when N=32 in Single Switch Faulty Condition.

Figure 4.67. Comparison of PP for IASEN-2, IAON and IASEN-3 when N=64 in Single Switch Faulty Condition.
Figure 4.68: Comparison of PP for IASEN-2, IAON and IASEN-3 when N=64 in Single Switch Faulty Condition.

Here the author has shown the simulation results of IASEN-2, IAON and IASEN-3 (from figure 4.40 to 4.68). Further he calculated the average PA which is as follows:

<table>
<thead>
<tr>
<th>Network</th>
<th>PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>IASEN-2</td>
<td>0.564</td>
</tr>
<tr>
<td>IAON</td>
<td>0.588</td>
</tr>
<tr>
<td>IASEN-3</td>
<td>0.714</td>
</tr>
</tbody>
</table>

Table 4.6

The table 4.4 clearly shows that the PA of IASEN-2 and IAON are 56.4% and 58.8% whereas PA of IASEN-3 is 71.4%.

It means IASEN-3 is 15% better than IASEN-2 and 12.6% better than IAON in terms of PA. Further, it is observed that performance of a network is primarily depending on the bandwidth because most of the factors of performance (e.g. TP, PU, PP) are calculated on the basis of bandwidth.
Therefore, the author has calculated the average bandwidth which is follows:

<table>
<thead>
<tr>
<th>N</th>
<th>IASEN-2</th>
<th>IAON</th>
<th>IASEN-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>9.032</td>
<td>9.420</td>
<td>11.438</td>
</tr>
<tr>
<td>32</td>
<td>18.065</td>
<td>18.840</td>
<td>22.877</td>
</tr>
<tr>
<td>64</td>
<td>36.130</td>
<td>37.680</td>
<td>45.754</td>
</tr>
<tr>
<td>128</td>
<td>72.261</td>
<td>75.360</td>
<td>91.508</td>
</tr>
</tbody>
</table>

Table 4.7

From table 4.5, it is observed that when size of network is doubled then value of bandwidth also gets doubled. So,

For IASEN-2=>

\[
\left( \frac{9.032}{16} \right) \times 100 = 56.4\%
\]

Here the size of network is 16 hence the author has taken the value 16 in denominator and multiplied by 100 to calculate the percentage.

For IAON=>

\[
\left( \frac{9.420}{16} \right) \times 100 = 58.8\%
\]

For IASEN-3=>

\[
\left( \frac{11.438}{16} \right) \times 100 = 71.4\%
\]

Again, it is observed that IASEN-3 is 15% better than IASEN-2 and 12.6% better than IASEN-2.

4.5.24 Throughput for IAON in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions

In figure 4.69, 4.70, 4.71 and 4.72, the author has shown the throughput of IAON for N=16, 32, 64 and 128 respectively. Here the throughput is calculated in non-faulty, single switch faulty and double switch faulty condition. Although, the throughput is decreasing in faulty conditions still it performs well in these conditions.
Figure 4.69. Comparison of TP for IAON when N=16 in Non-Faulty, Single Switch Faulty, and Double Switch Faulty Conditions.

Figure 4.70. Comparison of TP for IAON when N=32, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.
4.5.25 Processor Utilization for IAON in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions

In figure 4.73, 4.74, 4.75 and 4.76, the author has shown the processor utilization of IAON for N=16, 32, 64 and 128 respectively. Here the processor...
utilization is calculated in non-faulty, single switch faulty and double switch faulty condition. Although, the processor utilization is decreasing in faulty conditions still it performs well in these conditions.

Figure 4.73. Comparison of PU for IAON when N=16, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.

Figure 4.74. Comparison of PU for IAON when N=32, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.
Figure 4.75. Comparison of PU for IAON when N=64, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.

Figure 4.76. Comparison of PU for IAON when N=128, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.
4.5.26 Processing Power for IAON in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions

In figure 4.77, 4.78, 4.79 and 4.80, the author has shown the processing power of IAON for N=16, 32, 64 and 128 respectively. Here the processing power is calculated in non-faulty, single switch faulty and double switch faulty condition. Although, the processing power is decreasing in faulty conditions still it performs well in these conditions.

Figure 4.77. Comparison of PP for IAON when N=16, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.

Figure 4.78. Comparison of PP for IAON when N=32, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.
Figure 4.79. Comparison of PP for IAON when N=64, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.

Figure 4.80. Comparison of PP for IAON when N=128, in Non-Faulty, Single Switch Faulty and Double Switch Faulty Conditions.
4.6 Conclusion and Future Scope of the Work

In this chapter, the author has proposed two new fault tolerant network models named as irregular advance omega network and irregular augmented shuffle exchange network-3. The explanation of routing algorithms and theorems of IAON and IASEN-3 illustrates that all the proposed networks are good in terms of fault sustainability and performance. The performance of all the networks is based on bandwidth, the probability of acceptance, throughput, processor utilization and processing power.

IAON and IASEN-3 gives better performance than the MALN and IASEN-2 in non-faulty and single switch faulty conditions. Further, it is observed that IASEN-3 has better performance than IAON. However, IAON has double switch faulty tolerability and IASEN-3 has single switch fault tolerability. Performance of IAON is also calculated in double switch faulty case. It has been observed that in faulty conditions, the performance of each network is degraded. However, all the proposed MINs are still performing well in faulty situations than the earlier proposed MINs. In future, the author wants to apply new connection pattern on IAON and IASEN-3 so that both the networks can work effectively in crucial faulty situations.