Chapter 2

Two-Dimensional Analytical Model for Cylindrical Gate All Around (GAA) MOSFET Including Localized Charges

2.1 Introduction

This chapter illustrates the impact of hot carrier/process/radiation damage induced localized charges on the electrical performance of the cylindrical Gate All Around (GAA) MOSFET. As it has been seen in Chapter-1, GAA MOSFET also known as surrounding gate MOSFET and nanowire MOSFET, is one of the most promising device architecture to extend the scaling of the CMOS device as it provides the best electrostatic control of the channel [Auth97, Oh00]. Due to better gate control, GAA MOSFET is superior over Bulk MOSFET in terms of hot carrier reliability because of reduced short channel effects. A lot of research work is being carried out on fabrication techniques [Singh06] and analytical modeling [Chiang05, Moldovan07, Tsormpatzoglou09, Chiang09] of GAA MOSFET. Device reliability is also an important issue for nanoscale devices. With the increasing integration density of integrated circuits and reduction of dimensions of the device, probability of generation of interface traps/charges is very high and these charges have adverse effects on the device performance.

Device performance degradation due to interface traps induced at the Si-SiO₂ interface raises serious device reliability issues. These interface traps are generated due to: (1) process/stress induced damage [Poindexter89, Trabzon98], (2) radiation induced damage [Lho05] and (3) hot carrier induced damage [Shabde88, Naseh06]. For interface acceptor-type traps which appear at the Si-SiO₂ interface, damaged region will accept an electron if the trap level is located beneath the Fermi level. In this situation, damaged
region acts as negative fixed charge \([Shabde88]\). Similarly, a donor type interface trap acts as a positive localized interface charge. Therefore, induced interface traps can be treated as effective interface localized charges.

In the past, a lot of research work has been carried out on hot-carrier degradation of conventional MOS transistors \([Ng83, Hofmann85, Shabde88]\) and \([Jean97, Doyle90a, Doyle90b, Rafi99]\). Recently hot carrier effect has been studied in SOI MOSFET \([Jang08, Exarchos09]\). The effect of localized charges on electrical performance of the GAA MOSFET has been examined \([Djeffal09, Yu10, Abdi10, Chiang11]\) but most of them are limited to surface potential and threshold voltage modeling only and are based on parabolic potential profile approach. In this chapter, a two dimensional analytical model is developed for cylindrical GAA MOSFET including localized charges using evanescent mode analysis (EMA) technique which suits well for nanoscale GAA MOSFET having cylindrical gate. Cylindrical coordinates and Bessel function have been used to solve the Poisson’s equation, which is appropriate for finding the solution for the cylindrical geometry. The density of localized/fixed charges is chosen on the basis of various experimental studies which have been carried out in past to assess the performance degradation of MOSFET due to (a) hot carrier and stress damage \([Shabde88, Song93, Li97, Chim01, Sato11, Kim11, Vries12]\) resulting in density of interface states in the range of \(10^{10}-10^{13} \text{ cm}^{-2} \text{ eV}^{-1}\) (b) process damage \([Saks90]\) where interface states density is \(10^{10}-10^{11} \text{ cm}^{-2} \text{ eV}^{-1}\) (c) radiation damage \([Shanfield92]\) where trap density is \(10^{11}-10^{12} \text{ cm}^{-2} \text{ eV}^{-1}\). Distribution of the localized charges at the interface is considered to be uniform to make the analysis simple and easy to understand.

Further the effect of density of localized interface charges (both positive and negative), length of damaged region, and position of damaged region on the device characteristics (potential, conduction band energy, valence band energy, threshold voltage, subthreshold current and subthreshold slope) is analyzed. Apart from giving an estimation of performance degradation due to localized charges, the analytical results presented in this chapter are useful in predicting compact subthreshold modeling of GAA MOSFET including localized charges. The chapter also deals with the impact of localized charges
on the temperature sensitivity of the GAA MOSFET. The thermal characterization of a device is essential when the device is scaled down and operated over a large temperature range. Many papers have been reported on temperature analysis of MOSFET [Huang90, Chen96] and GAA MOSFET [Kranti99, Cho10]. However, impact of interface localized charges on the temperature sensitivity of the GAA MOSFET has been explored for the first time in this dissertation. The aim is to establish a relationship between the device degradation due to localized charges and temperature while explaining the factors affecting it.

2.2 Device Structure and Simulation Models

Fig. 2.01 shows the schematic 3-D and 2-D cross section of the nanoscale cylindrical GAA MOSFET structure with localized interface charges simulated using 3-D device simulator [Atlas10].

Figure. 2.01  (a) Simulated 3-D structure of cylindrical GAA MOSFET. (b) Schematic cross section of the simulated cylindrical GAA MOSFET. Device parameters are: Channel Length (L)=70 nm, Oxide thickness (t_{ox})=1.5 nm, Radius of Silicon pillar (R)=15 nm, Source/Drain doping (N_d)=1x10^{26} m^{-3}, Substrate Doping (N_a)=1x10^{21} m^{-3}, Gate Metal workfunction (\Phi_m)=4.5 eV. [Gautam12a]
The extension and position of localized charges is specified in terms of $L_2$ and $L_3$. $L_2$ denotes the length of damaged region where localized charges are present on the interface and $L_3$ denotes the distance of the damaged region from the drain end. The models activated in simulation comprise of field dependent mobility model, concentration dependent mobility model along with the Shockley–Read–Hall (SRH) recombination models for minority carrier recombination. For radius of the silicon pillar (R) greater than 5nm, quantum mechanical effects (QME) can be neglected [Tsormpatzoglou09] without compromising the accuracy of the results. Density of localized charges has been set using the parameter QF in the INTERFACE statement.

2.3 Two Dimensional Analytical Subthreshold Model

Evanescent-mode analysis is a powerful method for understanding short-channel effects. It properly deals with the two-dimensional (2-D) nature of the electrostatics and provides qualitatively different scaling predictions than analysis based on the parabolic approximation. To solve for potential distribution in silicon film, Poisson’s equation in cylindrical coordinates is written as [Chiang05]:

$$\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi(r,z)}{\partial r} \right) + \frac{\partial^2 \phi(r,z)}{\partial z^2} = \frac{q N_a}{\varepsilon_{si}}$$

(2.01)

where $\phi(r,z)$ is the two dimensional potential distribution in the silicon film, $N_a$ is the doping in the silicon film, $q$ is the electron charge and $\varepsilon_{si}$ is the dielectric permittivity of silicon. The two dimensional potential distribution $\phi(r,z)$ can be obtained using superposition technique. The potential, $\phi(r,z)$ is divided into two parts: long channel solution $V(r)$ to the Poisson's equation and short channel solution $U(r,z)$ to the Laplace equation. i.e.

$\phi(r,z) = V(r) + U(r,z)$

Thus eqn. (2.01) becomes:
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\[ \frac{1}{r} \frac{\partial V(r)}{\partial r} + \frac{\partial^2 V(r)}{\partial r^2} = \frac{qN_d}{\varepsilon_{si}} \quad (2.02) \]

\[ \frac{1}{r} \frac{\partial U(r,z)}{\partial r} + \frac{\partial^2 U(r,z)}{\partial r^2} + \frac{\partial^2 U(r,z)}{\partial z^2} = 0 \quad (2.03) \]

The boundary conditions required for the solution of two dimensional potential \( \phi(r,z) \) are as follows.

1. The center potential is a function of \( z \) only:
   \[ \phi(r = 0, z) = \phi_c(z) \quad (2.04a) \]

2. The electric field at the center of silicon film is zero:
   \[ \left. \frac{d\phi(r,z)}{dr} \right|_{r = 0} = 0 \quad (2.04b) \]

3. The electric field at the silicon oxide interface is given by:
   \[ \left. \frac{d\phi(r,z)}{dr} \right|_{r = \frac{t_{si}}{2}} = \beta \left[ V_{gs} - V_{fb} - \phi \left( r = \frac{t_{si}}{2}, z \right) \right] \quad (2.04c) \]

   where \( \beta = \frac{C_{oxcyl}}{\varepsilon_{si}} \quad (2.05a) \)

where \( V_{fb} \) is the flat band voltage of the damage free region, \( C_{oxcyl} \) is the gate oxide capacitance per unit area of the cylindrical-gate MOSFET, and is given as:

\[ C_{oxcyl} = \frac{2\varepsilon_{ox}}{t_{si} \ln \left( 1 + \left( \frac{2t_{ox}}{r_{si}} \right) \right)} \quad (2.05b) \]

\( \phi_c(z) \) is the potential at the center of the silicon film, \( V_{gs} \) is the gate to source voltage, \( \varepsilon_{ox} \) is the dielectric permittivity of oxide, \( t_{si} \) is the silicon film thickness, and \( t_{ox} \) is the oxide layer thickness. In order to study the effect of location and extension of localized charges on the electrical performance of the GAA MOSFET, channel region is divided into three
regions and the surface potential is obtained by solving the two-dimensional (2-D) Poisson’s equation separately in three regions and applying potential and field continuity conditions at interface of three regions, i.e. $L_2$ (length of damaged region), $L_3$ (distance of damaged region from drain), $L_4$ (damage free part i.e. $L-L_2-L_3$). Now $V_{fbi}$ can be written for three regions as [Gautam12a]:

$$V_{fbi} = \begin{cases} 
V_{fbi} & = V_{fb} 
& \text{for } i = 1, \quad 0 \leq z \leq L_1 \\
V_{fbi} & = V_{fb} - \frac{qN_f}{C_{ox}} 
& \text{for } i = 2, \quad L_1 \leq z \leq L_1 + L_2 \\
V_{fbi} & = V_{fb} 
& \text{for } i = 3, \quad L_1 + L_2 \leq z \leq L 
\end{cases}$$

(2.05c)

Here $N_f$ is the density of localized charges which can be positive or negative and $V_{fbi}$ is the flat band voltage for three different regions as shown in Fig. 2.01.

As the interface trap appears at the Si-SiO$_2$ interface, it is known that it will accept an electron if the trap level locates beneath the Fermi level for an acceptor-type interface trap. In this situation, it acts as negative interface fixed charge. Therefore, it can be approximated to equivalent interface fixed charge by [Jean97]

$$N_f = \frac{E_{Finv}}{E_V - E_{Finv}} \int D_{it}(E) dE$$

(2.06)

where $D_{it}$ is the interface trap density per energy interval per area, $E_V$ is the energy level of valence band, $E_{Finv}$ is the Fermi level as the device is operated at threshold voltage, and can be expressed as:

$$E_{Finv} = E_V + \frac{E_G}{2} + \frac{kT}{q} \ln \frac{N_A}{n_l}$$

(2.07)

where $E_G$ is the bandgap of silicon. For a donor-type interface trap, eqn. (2.06) will be integrated from $E_{Finv}$ to $E_C$ (energy level of conduction band) and it acts as positive interface fixed charge. However, $E_V$ in eqn. (2.07) should be replaced by $E_C$ and positive sign will be replaced by negative sign. Similarly, the oxide trapped charge can be treated as equivalent interface fixed charge if it located near the Si-SiO$_2$ interface. Using this simple transformation as described above, this model can be extended to all general cases for hot-carrier/stress/process damage/radiation damage induced damages.

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Solution of eqn. (2.02) using boundary conditions (2.04a)-(2.04c) can be expressed as:

\[ V_i(r) = \frac{qN_a r^2}{4\varepsilon_{si}} + V_{gs} - V_{fbi} - \frac{qN_a t_{si}^2}{4\varepsilon_{si} \beta} \]

(2.08)

The general solution of the Laplace equation in cylindrical coordinates is given by:

\[ U(r, z, \phi) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} J_m(k_{mn}r) \left( A_{mn} e^{k_{mn}z} + B_{mn} e^{-k_{mn}z} \right) \left( C_{mn} \cos m\phi + D_{mn} \sin m\phi \right) \]

(2.09)

Where \( J_m \) is the Bessel function of order \( m \) [Kreyszig93] and \( A \)'s, \( B \)'s, \( C \)'s and \( D \)'s are constants to be determined from boundary conditions.

Keeping only terms with \( m = 0 \) (since the potential cannot depend on \( \phi \) due to cylindrical symmetry) it can be written as:

\[ U_i(r, z) = \sum_{n=0}^{\infty} J_0(k_n r) \left( A_{ni} e^{k_{ni} z} + B_{ni} e^{-k_{ni} z} \right) \text{ for } i = 1, 2, 3 \]

(2.10)

where \( k_n = \frac{1}{\lambda_n} \) are the eigenvalues of

\[ J_1 \left( \frac{l_{si}}{2\lambda_n} \right) = \lambda_n \beta J_0 \left( \frac{l_{si}}{2\lambda_n} \right) \]

(2.11)

Due to rapid decay of the Bessel Fourier series coefficients, the first term is dominant and the two dimensional potential for the three regions can be expressed as:

\[ \phi_i(r, z) = \frac{qN_a r^2}{4\varepsilon_{si}} + V_{gs} - V_{fbi} - \frac{qN_a t_{si}^2}{4\varepsilon_{si} \beta} \frac{qN_a t_{si}^2}{16\varepsilon_{si}} + J_0(kr) \left( A_i e^{k_z} + B_i e^{-k_z} \right) \]

(2.12)

Where \( A_i \) and \( B_i \) are calculated by applying continuity of surface potential and electric field at interfaces of damaged and damage free regions, i.e.,

\[ \phi_1(r, L_1) = \phi_2(r, L_4) \]

(2.13a)

\[ \phi_1(r, L_1+L_2) = \phi_2(r, L_1+L_2) \]

(2.13b)

\[ \phi_1'(r, L_1) = \phi_2'(r, L_1) \]

(2.13c)

\[ \phi_1'(r, L_1+L_2) = \phi_2'(r, L_1+L_2) \]

(2.13d)

and the boundary conditions at the source and drain edges are
\[ \varphi_1(r,0) = V_{bi} \]  
(2.13e)

\[ \varphi_3(r,L) = V_{bi} + V_{ds} \]  
(2.13f)

where \( V_{bi} \) is the built-in potential of the source/drain junction and \( V_{ds} \) is the drain to source voltage. Applying these conditions in eqn. (2.12), gives following expressions for the coefficients [Gautam12a]:

\[ \phi_i = V_{gs} - V_{fbi} - \frac{qN_{a}t_{si}}{4\varepsilon_{si}} - \frac{qN_{a}^2 t_{si}^2}{16\varepsilon_{si}} \]  
(2.14)

\[ A_1 = \left( V_{bi} \frac{RJ_1(kR)}{kX} - P \right) e^{-kL_1} + A_2 e^{kL_1} - B_2 e^{-kL_1} \]  
\[ \frac{2 \cosh(kL_1)}{} \]  
(2.15)

\[ B_1 = \left( V_{bi} \frac{RJ_1(kR)}{kX} - P \right) e^{kL_1} - A_2 e^{-kL_1} + B_2 e^{kL_1} \]  
\[ \frac{2 \cosh(kL_1)}{} \]  
(2.16)

\[ A_3 = \left( V_{bi} + V_{ds} \right) \frac{RJ_1(kR)}{kX} - P \right) e^{-k(L_1+L_2)} + \left( A_2 e^{k(L_1+L_2)} - B_2 e^{-k(L_1+L_2)} \right) e^{-kL} \]  
\[ \frac{2 \cosh(kL_3)}{} \]  
(2.17)

\[ B_3 = \left( V_{bi} + V_{ds} \right) \frac{RJ_1(kR)}{kX} - P \right) e^{k(L_1+L_2)} - \left( A_2 e^{k(L_1+L_2)} - B_2 e^{-k(L_1+L_2)} \right) e^{kL} \]  
\[ \frac{2 \cosh(kL_3)}{} \]  
(2.18)

Where

\[ A_2 = \frac{b_3 b_5 - b_2 b_6}{b_1 c_5 - b_2 b_4} \]  
(2.19)

\[ B_2 = \frac{b_1 b_6 - b_3 b_4}{b_1 c_5 - b_2 b_4} \]  
(2.20)

\[ b_1 = \left(1 - \tanh(kL_1)\right) e^{kL_1} \]  
(2.21)

\[ b_2 = \left(1 + \tanh(kL_1)\right) e^{-kL_1} \]  
(2.22)
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\[ b_3 = P - Q + \frac{V_{b1}}{kX} \frac{R J_1 (kR)}{\cosh k L_1} - P \] (2.23)

\[ b_4 = \left(1 + \tanh k L_3\right) e^{k(L_1+L_2)} \] (2.24)

\[ b_5 = \left(1 - \tanh k L_3\right) e^{-k(L_1+L_2)} \] (2.25)

\[ b_6 = P - Q + \frac{(V_{ds}+V_{bi})}{kX} \frac{R J_1 (kR)}{\cosh k L_3} - P \] (2.26)

\[ X = \frac{R^2 J_0^2 (kR)}{2} + \frac{R^2 J_1^2 (kR)}{2} \] (2.27)

\[ P = \frac{\phi_1 R J_1 (kR)}{kX} + \frac{q N_a}{\varepsilon_{si}} \left( k R^3 J_1 (kR) + 2 R^2 J_2 (kR) \right) \] (2.28)

\[ Q = \frac{\phi_2 R J_1 (kR)}{kX} + \frac{q N_a}{\varepsilon_{si}} \left( k R^3 J_1 (kR) + 2 R^2 J_2 (kR) \right) \] (2.29)

Continuous two dimensional potential for the complete channel length can be written as:

\[ \phi(r,z) = \begin{cases} 
\phi_1(r,z) & 0 \leq z \leq L_1 \\
\phi_2(r,z) & L_1 \leq z \leq L_1 + L_2 \\
\phi_3(r,z) & L_1 + L_2 \leq z \leq L 
\end{cases} \] (2.30)

2.3.1 Impact of Localized Charges on Flat Band Voltage and Surface Potential

The effect of immobile/localized charges at the interface of oxide and semiconductor is such that additional band bending takes place due to these localized charges which results in change in flat band voltage in the damaged region. Fig. 2.02 illustrates this change in band bending in terms of conduction and valence band energies as a function of position.
along the channel. As can be seen from Fig. 2.02, as the conduction band and valance band energy is raised (lowered) in the damaged region for negative (positive) localized charges, there is a change in the flat band voltage in the damaged region.

Figure 2.02 Conduction and valence band energy as a function of distance along the channel. Other parameters are \( V_{gs} = 0 \) V, \( V_{ds} = 0 \) V, \( L = 70 \) nm, \( t_{ox} = 1.5 \) nm, \( R = 15 \) nm, \( N_d = 1 \times 10^{26} \) m\(^{-3}\), \( N_a = 1 \times 10^{21} \) m\(^{-3}\). [Gautam12a]

The amount of change in the flat band voltage \( \Delta V_{fb} \) depends upon the thickness of the gate oxide \( t_{ox} \), permittivity of the oxide \( \varepsilon_{ox} \), and density of localized charges \( N_f \) and is given by [Arora93]:

\[
\Delta V_{fb} = \frac{qN_f}{C_{oxyl}}
\] (2.31)

By setting the first derivative of eqn. (2.12) at \( r = t_{si}/2 \) to zero, the minimum surface potential and its position can be expressed as:

\[
\varphi_{\text{min}i} = V_{gs} - V_{fbi} - \frac{qN_d t_{si}}{4\varepsilon_{si}\beta} + 2J_0 \left( \frac{t_{si}}{2} \right) \sqrt{A_i B_i}
\]

\[
z_{\text{min}i} = \frac{1}{2k} \ln \left( \frac{B_i}{A_i} \right)
\]  

\( i = 1, 2, 3 \)  

(2.32)
For negative (positive) localized charges the surface potential is lowered (increased) in the damaged region because the flat band voltage \( V_{fb} \) in the damaged region increases (decreases) depending on the nature of localized charges. Fig. 2.03 shows the simulated surface potential contour plot for channel length, \( L=32 \text{nm} \). Here positive localized charges are present near the drain end where potential is lowered as shown in Fig. 2.03. Here pink colour represents the potential in the damaged region which is lower than the potential in the undamaged region represented by blue colour in the figure.

![Simulated contour surface potential plot](image)

**Figure. 2.03** Simulated contour surface potential plot as a function of distance along the channel for GAA MOSFET having localized charges. Other parameters are \( V_{gs}=0 \text{ V}, \ V_{ds}=0 \text{ V}, \ L=32 \text{ nm}, \ L_2=16 \text{ nm}, \ L_3=4 \text{ nm}, \ t_{ox}=1.5 \text{ nm}, \ R=5 \text{ nm}, \ N_d=1 \times 10^{26} \text{ m}^{-3}, \ N_a=1 \times 10^{21} \text{ m}^{-3}. \) [Gautam12b]

Fig. 2.04 shows variation in surface potential profile with localized charges for various lengths of damaged region. In case of the negative (positive) interface localized charges, the minimum surface potential appears in the damaged (undamaged) region. Thus localized charges result in the shift in the minimum surface potential. When localized charges are induced due to hot carrier effect they are generally located near the drain \[Shabde88, Djeffal09\]. But if the localized charges are induced due to radiation damage \[Shanfield92\], plasma etching \[Trabzon98\] or stress induced \[Doyle90a, Doyle90b\], they may occur anywhere at the Si-SiO\(_2\) interface near the source side also. Incident radiation \[Shanfield92\] results in the formation of an electron-hole pair (EHP). The radiation induced electrons are much more mobile than the holes and are swept out of the oxide.
layer very fast under the influence of strong transverse electric field. The holes that are relatively immobile result in a negative shift of the flat band voltage. Thus, radiation induced damage generally increases the positive oxide charge density and interface state density which causes device threshold voltage shift and reduce channel transconductance. Similarly stress induced damage causes charge trapping in the gate

Figure. 2.04 Surface potential along the channel for various lengths of damaged region. Device parameters are $V_{gs}=0$ V, $V_{ds}=0$ V, $L=70$ nm, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1\times10^{26}$ m$^{-3}$, $N_a=1\times10^{21}$ m$^{-3}$. [Gautam11b], [Gautam12a].
oxide and interface states generation at the interface [Doyle90b]. Fig. 2.05 illustrates the behavior of localized charges located at the source side. So, when the damaged region is near the drain side and has positive fixed charges, it screens the undamaged region from the drain bias. On the other hand when the damaged region having negative fixed charges is near the source side, undamaged region screens the damaged region. Thus, behavior of the device having positive (negative) localized charges at higher drain to source bias will be different from the case of undamaged device.

Figure. 2.05 Surface potential along the channel when damaged region is located near the source side. Device parameters are $V_{gs}=0$ V, $V_{ds}=0$ V, $L=70$ nm, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1x10^{26}$ m$^{-3}$, $N_a=1x10^{21}$ m$^{-3}$ [Gautam11b], [Gautam12a].

Fig. 2.06 illustrates the impact of increasing the density of localized charges on the surface potential. As can be seen from the figure, value of minimum surface potential and its position remains nearly unchanged as density of positive localized charges is increased. Thus, in case of positive localized charges, source side is screened from the effect of applied drain to source bias at the drain side. On the other hand, there is a significant change in minimum surface potential value and its position in case of negative localized charges which will lead to greater variation in threshold voltage and drain current. Therefore, variation in the device characteristics due to negative localized charges will be more as compared to positive localized charges.
2.3.2 Impact of Localized Charges on Subthreshold Current and Subthreshold Slope

High leakage current in nanoscale devices is a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Subthreshold current (i.e. weak inversion current) is the main contributor to the leakage current or off current ($I_{off}$) in the GAA MOSFET. It is important to keep $I_{off}$ very small in order to minimize the static power that a circuit consumes when it is in the standby mode. Therefore, modeling of subthreshold degradation due to localized charges is very important especially for digital low-power applications. Subthreshold drain current $I_{sub}$ can be evaluated by using eqn. (2.30) of surface potential as:

$$I_{sub} = 2 \pi \mu q \frac{n_i}{L} \left( \int_0^R \int_0^z e^{-qV(z)/kT} e^{q\varphi(r,z)/kT} dr \right) dz$$

(2.33)
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\[ I_{sub} = 2 \pi \mu k T n_i \frac{e^{-qV_s/kT} - e^{-qV_d/kT}}{L} dz \int_{0}^{L} \int_{0}^{R} q \varphi(r, z)/kT dr \] ...

(2.34)

Here \( V_{ds} \) is the drain to source voltage, \( n_i \) is the intrinsic carrier concentration, \( \mu \) is the low field or bulk mobility. Change in the charge distribution, flat band voltage and surface potential due to localized charges leads to degradation of subthreshold current and subthreshold slope. Positive (negative) localized charges result in the increase (decrease) of subthreshold current as shown in Fig. 2.07.

**Figure. 2.07** Subthreshold current as a function of gate to source voltage. Device parameters are: \( L=70 \) nm, \( t_{ox}=1.5 \) nm, \( R=15 \) nm, \( N_d=1x10^{26} \) m\(^{-3}\), \( N_a=1x10^{21} \) m\(^{-3}\). [Gautam12a]

Apart from subthreshold degradation, deviation introduced in the on current to off current ratio i.e. \( I_{on}/I_{off} \) due to localized charges is also important for switching applications where a high value of \( I_{on}/I_{off} \) is required. Poor \( I_{on}/I_{off} \) can cause slow output transitions or low output swings thus for logic applications, the \( I_{on}/I_{off} \) ratio should be as large as possible. For negative localized charges \( I_{on} \) (\( I_{off} \)) is decreased whereas for positive localized charges \( I_{on} \) (\( I_{off} \)) is increased as shown in the Fig. 2.08. Thus, positive localized charges increase both the \( I_{on} \) and \( I_{off} \) but the order of the increase in the \( I_{off} \) is much more than the \( I_{on} \). Thus, degradation due to localized charges is larger in subthreshold region. The overall result is that the \( I_{on}/I_{off} \) ratio is reduced from \( 1.9x10^4 \) to \( 6.8x10^3 \) for positive...
localized charges and increased from $1.9 \times 10^4$ to $9.1 \times 10^4$ for negative localized charges as shown in Fig. 2.09.

\[ \text{Figure. 2.08} \quad \text{Simulated Drain current as a function of gate to source voltage. Device parameters are: Length of damaged region } L_2 = 35 \text{ nm, Channel Length } L = 70 \text{ nm, } t_{ox} = 1.5 \text{ nm, } R = 15 \text{ nm, } N_d = 1 \times 10^{26} \text{ m}^{-3}, N_s = 1 \times 10^{21} \text{ m}^{-3}. [\text{Gautam11a}] \]

\[ \text{Figure. 2.09} \quad \text{Effect of localized charges on } I_{on}/I_{off} \text{ ratio. Device parameters are Length of damaged region } L_2 = 35 \text{ nm, Channel Length } L = 70 \text{ nm, } L_3 = 0, t_{ox} = 1.5 \text{ nm, } R = 15 \text{ nm, } N_d = 1 \times 10^{26} \text{ m}^{-3}, N_s = 1 \times 10^{21} \text{ m}^{-3}. [\text{Gautam11a}] \]

The leakage power is strongly influenced by the subthreshold swing or subthreshold slope of a device defined as:
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\[ S = \left[ \frac{d \log (I_{\text{sub}})}{dV_{\text{gs}}} \right]^{-1} \]  

(2.35)

where \( I_{ds} \) is the drain-to-source current under an applied gate-to-source voltage i.e. \( V_{gs} < V_{th} \) where \( V_{th} \) is the threshold voltage of the device. The subthreshold slope (\( S \)) indicates the minimum amount of gate-voltage reduction necessary to lower the subthreshold current by a factor of ten. A device characterized by steep subthreshold slope exhibits a faster transition between off (low current) and on (high current) states. Fig. 2.10 shows that subthreshold slope variation with channel length for both damaged and damage-free device. Subthreshold slope is more (less) in case of positive (negative) localized charges because of the enhancement (decrease) in the subthreshold current (i.e. off-current).

2.3.3 Impact of Localized Charges on Threshold Voltage and DIBL

Threshold voltage (gate to source voltage at which the device gets turn on) is another important parameter for digital and switching applications. From the modeling point of view, it is important as threshold voltage roll off is the most common method of measuring short channel effects present in the device. Since small geometry effects and localized charges cause variations in the threshold voltage, therefore, it is critical for circuit and device designers to be able to predict these variations. There are various methods reported to model the threshold voltage in GAA MOSFET such as virtual...
cathode method [Hamid07] and constant current method [Yan91], [Lu05]. In this work, subthreshold current has been calculated using constant current method. The threshold voltage is measured at the drain current of $6 \times 10^{-7}$ A. Due to the step in the surface potential profile the minimum surface potential lies in the damaged region in case of negative localized charges whereas in case of positive localized charges it lies in the undamaged region. For $1 \times 10^{16}$ m$^{-2}$ density of localized charges and length of damage region ($=L/2$), threshold voltage is reduced by 11.76 % (increased by 26.47 % ) in case of positive (negative ) localized charges and this change i.e. ($\Delta V_{th}$) increases as the density of localized charges is increased as shown in Fig. 2.11. The rate of change in threshold voltage ($\Delta V_{th}$) is more for negative localized charges as compared to positive charges because the minimum surface potential remains nearly unchanged for positive localized charges when density of localized charges is increased whereas for negative localized charges minimum surface potential is changed significantly with density of localized charges and its position (i.e. $x_{min}$) shifts more towards the source side as the length of damaged region is increased.

![Figure 2.11](image.png) Threshold voltage as a function of density of localized charges. Device parameters are: $L_2=35$ nm, $V_{ds}=0.05$ V, $L=70$ nm, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1\times10^{26}$ m$^{-3}$, $N_s=1\times10^{21}$ m$^{-3}$. [Gautam12a]
Fig. 2.12 shows the impact of length of damaged region on the threshold voltage. When damaged region’s length is small the change in threshold voltage is negligibly small but as the length of damaged region increases threshold voltage decreases (increases) for positive (negative) localized charges respectively because of greater change in band bending. Fig. 2.13 illustrates the impact of position of damaged region on the threshold voltage degradation due to localized charges. It is seen that maximum degradation occurs when localized charges are present in the middle of the Si-SiO₂ interface because in that position maximum change takes place in the minimum surface potential.
Fig. 2.14 (a) shows the effect of varying the radius of silicon pillar on the threshold voltage of undamaged and damaged device. As can be seen from the Fig. 2.14 (a), for both undamaged and damaged device the threshold voltage increases with decreasing silicon body radius because when the silicon pillar radius is thin the carrier population is confined into the vary narrow space where carriers are pushed away from the Si-SiO$_2$ interface and increases the threshold voltage. Increasing radius of silicon pillar ($R$) from 5 nm to 15 nm reduces the threshold voltage from 0.258 V to 0.17 V for undamaged device, 0.236 V to 0.15 V for positive localized charges and 0.3 V to 0.216 V for negative localized charges. Fig. 2.14 (b) shows threshold voltage reduction (for both undamaged and damaged devices) as the channel length decreases. The decrease in channel length reduces gate controlled channel charge thereby decreasing the threshold voltage. When channel length is reduced from 70 nm to 45 nm threshold voltage is reduced by 40 mV (50 mV) in case of positive (negative) localized charges.

![Figure 2.14](image)

**Figure. 2.14** Threshold voltage as a function of (a) radius of silicon pillar, (b) channel length. Device parameters are: $L_2=35$ nm, $V_{d}=0.05$ V, $L=70$ nm, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1\times10^{26}$ m$^{-3}$, $N_a=1\times10^{21}$ m$^{-3}$. [Gautam12a]

For sub-100 nm device dimensions, it is increasingly important to model SCEs such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off accurately. DIBL is caused by the encroachment of the depletion region from the drain into the channel. At
high drain bias, the depletion region strongly affects the channel potential. As a result, the threshold condition can be reached at a lower gate voltage since the drain has already created a large portion of the depletion region. The strength of DIBL is usually measured as the difference in $V_{th}$ between a low (50-100 mV) and a high ($V_{ds}$) drain bias. Strong DIBL is an indication of poor short-channel behavior. Table. 2.01 shows threshold voltage roll-off due to higher drain bias $\Delta V_{th} = V_{th}(V_{ds}=0.05\, V) - V_{th}(V_{ds}=0.5\, V)$ for both damaged and undamaged device. The positive (negative) charges near the drain (source) side effectively suppress the field penetration from the drain, thus, the threshold voltage reduction due to DIBL is reduced. Therefore, as shown in Table. 2.01, the reduction in threshold voltage due to higher drain to source voltage ($V_{ds}$) is less in case of positive (negative) localized charges lying near the drain (source) side because of the screening effect.

Table. 2.01
Threshold voltage roll-off due to higher drain bias for both damaged and undamaged device. Device parameters are $L_2=L/2$, $L=70$ nm, $R=15$ nm, $V_{ds}=0.05$ V, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1x10^{26}$ m$^{-3}$, $N_a=1x10^{21}$ m$^{-3}$, $\varepsilon_{ox}=3.9$. [Gautam12a]

<table>
<thead>
<tr>
<th>$L_2$ (nm)</th>
<th>$L_3$ (nm)</th>
<th>$N_f$ ($m^2$)</th>
<th>Simulated</th>
<th>Analytical</th>
</tr>
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<tr>
<td></td>
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<td>$V_{th}$</td>
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<td></td>
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<td></td>
<td>@ $V_{ds}$=0.05V</td>
<td>@ $V_{ds}$=0.5V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>170</td>
<td>156</td>
</tr>
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<tr>
<td>35</td>
<td>0</td>
<td>$-10^{16}$</td>
<td>215</td>
<td>190</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
<td>$-10^{16}$</td>
<td>222</td>
<td>210</td>
</tr>
</tbody>
</table>

Early voltage is also an important parameter to measure the channel length modulation (CLM) effect. Fig. 2.15 shows the effect of localized charges on the early voltage. As expected high value of early voltage is obtained for positive localized charges due to screening of the channel potential from higher drain bias.
Figure 2.15 Early voltage as a function of drain to source voltage. Device parameters are: $V_{gs}=0.4 \text{ V}$, $L=70 \text{ nm}$, $t_{ox}=1.5 \text{ nm}$, $R=15 \text{ nm}$, $N_d=1 \times 10^{26} \text{ m}^{-3}$, $N_a=1 \times 10^{21} \text{ m}^{-3}$. [Gautam11b]

2.3.4 Role of Device Dimensions

Fig. 2.16 (a)-(c) shows the effect of radius of silicon pillar on the subthreshold current for both undamaged and damaged device. As is clear from the figure that the thicker silicon body leads to higher $I_{off}$. For undamaged device, increasing silicon pillar radius ($R$) from 5 nm to 15 nm increases the $I_{off}$ from 0.061 nA to 1.27 nA.

Similarly for positive localized charges $I_{off}$ increases from 0.124 nA to 3.75 nA and for negative localized charges $I_{off}$ increases from 0.012 nA to 0.26 nA. However, regardless of higher subthreshold leakage, thicker silicon bodies provide higher driving current
which is proportional to the area $\pi t_{si}^2$. Thus, for applications where low off current is required, the device with smaller value of $R$ should be used. The trade-off between how to keep low subthreshold degradation and to have high driving capability should be accounted for simultaneously as the device is designed for the circuit applications. Also, the impact of localized charges on subthreshold current is higher for thicker device having larger radius of silicon body ($R = t_{si}/2$). This is because for greater radius ($R$), the oxide capacitance $C_{oxoy}$ (given by eqn. (2.05b)) is less which means greater change in flat band voltage (given by $qN_f/C_{oxoy}$), hence, greater sensitivity to localized charges. Fig. 2.17 shows the effect of oxide thickness on device degradation due to localized charges.

*Figure. 2.17* (a) Surface Potential as a function of position along the channel, (b) and (c) Subthreshold current as a function of gate to source voltage for two values of oxide thickness. Device parameters are: $L_2 = L/2$, $V_{gs} = 0$ V, $V_{ds} = 0.05$ V, $L = 70$ nm, $R = 15$ nm, $N_{d} = 1 \times 10^{26}$ m$^{-3}$, $N_{i} = 1 \times 10^{21}$ m$^{-3}$. 
In accordance with eqn. (2.31), amount of degradation due to localized charges directly depends on the thickness of the oxide layer. So when oxide thickness is increased from 1.5 nm to 3 nm, greater change in band bending give rise to larger degradation in surface potential and subthreshold current as shown in Fig. 2.17.

2.4 Effect of Temperature

2.4.1 Temperature Dependent Model

Temperature dependent modeling is important for designing circuits which must operate over a wide range of temperatures. Accurate description of temperature effects in a device having localized charges is necessary to predict variations caused by localized charges in the temperature sensitivity of the device and for this all of the temperature dependences need to be modelled correctly. In order to study the impact of localized charges on the temperature sensitivity of the device, temperature dependency of various temperature sensitive parameters like bandgap ($E_g$), intrinsic carrier concentration ($n_i$), dielectric constant of silicon ($\varepsilon_{si}$), fermi potential ($\Phi_f$), built-in-potential ($V_{bi}$), flatband voltage ($V_{fb}$) and mobility are incorporated in the analytical model derived in section 2.3 and are verified with the simulation results [Atlas10]. In simulation ANALYTIC mobility model is used to consider concentration and temperature dependent mobility and SURFMOB surface mobility degradation model is used to consider reduction of electron mobility due to Coulomb scattering. Analytical model derived in section 2.3 is modified to include various temperature dependent parameters as given below [Atlas10]:

$$E_g(T) = E_g(300) + E_g\alpha \left( \frac{300^2}{300 + E_g\beta} - \frac{T^2}{T + E_g\beta} \right)$$  \hspace{1cm} (2.36)

Here $E_g(300)$=1.08 eV, $E_g\alpha$=4.73x10$^{-4}$ eV/K, $E_g\beta$=636 K.

$$n_i(T) = 1.706 \times 10^{25} \left( \frac{T}{300} \right)^3 \left( \exp \left( \frac{-qE_g(T)}{kT} \right) \right)$$  \hspace{1cm} (2.37)

$$\varepsilon_{si}(T) = 11.40 + \left( 1 + 1.2 \times 10^{-4} T \right)$$  \hspace{1cm} (2.38)
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\[ \phi_f (T) = \frac{kT}{q} \ln \left( \frac{N_a}{n_i (T)} \right) \]  
(2.39)

\[ V_{bi} (T) = \frac{kT}{q} \ln \left( \frac{N_a N_d}{n_i^2 (T)} \right) \]  
(2.40)

\[ \phi_s (T) = \frac{E_g (T)}{2} + \chi - q\phi_f (T) \]  
(2.41)

\[ V_{fb} (T) = \phi_m - \phi_s (T) \pm \frac{qN_f}{C_{oxcy}} \]  
(2.42)

Using eqn. (2.36) to (2.42), a temperature dependent expression is obtained for two dimensional surface potential. Fig. 2.18 illustrates the impact of localized charges on surface potential at various temperatures for an undamaged device, damaged device having positive localized charges and damaged device having negative localized charges. As can be seen from Fig. 2.18 as temperature is decreased, minimum surface potential is increased by few mV but at the same time intrinsic carrier concentration is also decreased and the order of change in \( n_i \) is much greater than change in surface potential. Thus, as temperature is decreased, decrease in intrinsic carrier concentration dominates over increase in minimum surface potential thereby leading to decrease in subthreshold current and increase in threshold voltage. The temperature dependent two dimensional potential is used to calculate the drain current in subthreshold region as:

\[ I_{sub} = \frac{2\pi R_{\mu eff} qn_i}{V_s} \int V_d \frac{-qV(z)}{e^{kT} dV} dz \]  
(2.43)

where effective mobility \( (\mu_{eff}) \) is calculated by applying Mathiessen’s law as follows:

\[ \frac{1}{\mu_{eff}} = \frac{1}{\mu_o} + \frac{1}{\mu_{Caug}} \]  
\( 0 \leq z \leq L_1, \ L_1 + L_2 \leq z \leq L \)  
(2.44)
\[
\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_0} + \frac{1}{\mu_{\text{ox}}} + \frac{1}{\mu_{\text{Caug}}} \quad L_1 \leq z \leq L_1 + L_2
\] (2.45)

where \(\mu_0\) is defined as the bulk mobility or the low field mobility.

Figure 2.18 Surface potential as a function of position along the channel of GAA MOSFET for (a) undamaged device, (b) damaged device having positive localized charges and (c) damaged device having negative localized charges. Device parameters: Channel Length (L) = 50 nm, Radius (R) = 10 nm, Length of damaged region (L_2) = L, Oxide thickness (t_{ox}) = 2 nm, Metal workfunction (\(\varphi_m\)) = 4.4 eV, Source/drain doping (N_d) = 1x10^{26} m^{-3}, Substrate doping (N_a) = 1x10^{21} m^{-3}. [Gautam13]

An important effect of the hot-carrier induced localized interface charge density is the reduction of electrons mobility due to Coulomb scattering. Oxide-interface charge scattering mobility is given by [Nishida87, Leblebici92]:

\[ \text{[Details about mobility reduction due to Coulomb scattering provided here.]} \]
Another important effect is mobility variation with temperature. Caughey and Thomas analytic function [Caughey67] is used to model temperature dependent mobility given by:

\[
\mu_{\text{Caug}} = \mu_1 + \frac{\mu_2 \left( \frac{T}{300} \right)^\beta}{1 + \left( \frac{T}{300} \right)^\gamma \left( \frac{N_a}{N_{\text{crit}}} \right)^\delta}
\]  

(2.47)

where parameters are: \( \mu_1 = 55.24 \ \text{cm}^2/\text{Vs}, \ \mu_2 = 240 \ \text{cm}^2/\text{Vs}, \ \beta = -2.3, \ \gamma = -3.8, \ N_{\text{crit}} = 1.072 \times 10^{17} \ \text{cm}^{-3} \). The electric field and mobility are also affected due to the presence of localized charges in the damaged device leading to change in carrier velocity profile thereby affecting the drain current. Fig. 2.19 shows the impact of temperature on the subthreshold current for undamaged device and damaged device having positive and negative localized charges. The temperature coefficient of the drain current \( (I_{ds}) \) is positive, negative or zero depending upon the operating voltage. The positive temperature coefficient of \( I_{ds} \) (\( I_{ds} \) increases as temperature increases) occurs when the device is operating in the subthreshold and weak inversion region which is due to increase in intrinsic carrier concentration with increase in temperature. However, in saturation region \( I_{ds} \) has a negative temperature coefficient. The negative temperature coefficient of \( I_{ds} \) at higher temperatures is primarily due to decrease in the carrier mobility. One more parameter affected due to localized charges is zero crossover point (ZCP) which is the gate voltage at which the temperature coefficient of the drain current is zero as shown in Fig. 2.20. Fig. 2.20 (a) and (b) demonstrate the change in \( I_{\text{off}} \) and \( I_{\text{on}} \) as a function of temperature where change in \( I_{\text{off}} \) (\( I_{\text{on}} \)) is exponential (linear) with increase in temperature.
As can be seen from Fig. 2.19 and Fig. 2.20, variations caused due to localized charges and temperature are more prominent in subthreshold region due to larger carrier screening length in subthreshold region as suggested by Gao et.al. [Gao10]. It is also shown that subthreshold degradation due to localized charges is greater at low temperatures, thus impact of localized charges can be suppressed at higher temperatures.
From the subthreshold current, threshold voltage is calculated using constant current method (i.e. $V_{gs}$ corresponding to $I_{ds}=6\times10^{-7}$ A). As temperature increases threshold voltage decreases for both undamaged and damaged device as shown in Fig. 2.21. For both undamaged and damaged devices the temperature dependence of threshold voltage can be attributed to temperature sensitive parameters like bandgap, built-in-potential, Fermi potential, flatband voltage, intrinsic carrier concentration. As it has been seen in Fig. 2.18, that as temperature is decreased, minimum surface potential is increased (by few mV) which should decrease the threshold voltage but other parameters such as intrinsic carrier concentration decreases exponentially and thus dominates over potential leading to increase in threshold voltage with decrease in temperature.

![Figure 2.20](image1.png)  
**Figure. 2.20**  
(a) $I_{off}$  (b) $I_{on}$ as a function of temperature for GAA MOSFET. Device parameters: $L=50$ nm, $R=10$ nm, $L_2=L$, $t_{ox}=2$ nm, $\phi_m=4.4$ eV, $N_d=1\times10^{26}$ m$^{-3}$, $N_a=1\times10^{21}$ m$^{-3}$. [Gautam13]

![Figure 2.21](image2.png)  
**Figure. 2.21**  
Threshold voltage as a function of temperature. Device parameters: $L=70$ nm, $L_1=L_2=L/2$, $t_{ox}=1.5$ nm, $R=15$ nm, $N_d=1\times10^{26}$ m$^{-3}$, $N_a=1\times10^{21}$ m$^{-3}$, $V_{ds}=0.05$ V. [Gautam11c]
2.4.2 Impact of Localized Charges on Temperature Sensitivity

It has been shown that localized charges not only degrade the subthreshold characteristics of the device but it also changes the temperature sensitivity of the device. To study the impact on temperature sensitivity, a sensitivity parameter $S_T$ can be defined as:

$$S_T = \left( \frac{\partial \log(I_{off})}{\partial T \text{ (in K)}} \right)^{-1} \text{ K/Dec}$$

(2.48)

$S_T$ can be calculated from the slope of the $I_{off}$ versus temperature ($T$) curve in Fig. 2.20. Table 2.02 shows the impact of localized charges on the sensitivity parameter $S_T$ and zero crossover point.

**Table. 2.02**

Impact of localized charges on the temperature sensitivity of GAA MOSFET. Device parameters: $L=50$ nm, $R=10$ nm, $L_2=L$, $t_{ox}=2$ nm, $\varphi_m=4.4$ eV, $N_d=1x10^{26}$ m$^{-3}$, $N_a=1x10^{21}$ m$^{-3}$. [Gautam13]

<table>
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<tr>
<th></th>
<th>For undamaged device</th>
<th>For $N_F=10^{16}$ m$^{-2}$</th>
<th>For $N_F=-10^{16}$ m$^{-2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_T$ (K/Dec)</td>
<td>24</td>
<td>35</td>
<td>18</td>
</tr>
<tr>
<td>ZCP (V)</td>
<td>0.25</td>
<td>0.19</td>
<td>0.34</td>
</tr>
</tbody>
</table>

As is clear from the Table 2.02, change of 24 K in temperature changes the $I_{off}$ by a factor of 10 for undamaged device whereas for damaged device having positive (negative) localized charges, for a decade change in $I_{off}$, 35 K (18 K) change in temperature is required. Thus, positive (negative) localized charges lead to enhanced (reduced) temperature sensitivity of the device. Also the zero crossover point is shifted about 30% in presence of localized charges. Significance of zero crossover point is that if the device is to be used for temperature invariant applications, it should be biased at this zero crossover point where change in drain current due to change in temperature is zero. Thus, zero crossover point is the optimum bias point for a device for temperature invariant applications and its value gets changed in presence of damage induced localized charges.
2.5 Summary
For projecting the performance degradation due to hot carrier damage/radiation damage/process damage induced localized charges in future nanometer device dimensions, accurate analytical model is very important. In this chapter, a new simple and computationally efficient two-dimensional analytical model that can accurately models GAA MOSFET having cylindrical geometry incorporating the effect of interface localized charges has been presented and verified. Applying the constraints of potential and electric field continuity, combined with the boundary conditions in the source and drain boundaries, the surface potential and subthreshold current model is obtained. Further, an analytical drain current model has been developed using charge control model applicable to channel radius less than 5 nm. It includes quantum effects, velocity overshoot effects and channel length modulation effects which become very important when channel radius is scaled below 5 nm and channel length below 40 nm. The model compares well with simulated data and shall be useful in estimation of performance degradation due to localized charges. Presence of localized charges at Si-SiO₂ interface causes a step in the potential profile which results in the shift of threshold voltage, degradation of subthreshold current and subthreshold slope of the device. The analytical results are verified with the simulated results and it can be concluded from the results that negative (positive) localized charges leads to increase (decrease) in threshold voltage and decrease (increase) in subthreshold current and subthreshold slope of the device. Results show that localized charges mainly degrade the subthreshold characteristics of the device. Also the impact of variation in channel length, channel radius, oxide thickness on performance degradation due to localized charges is studied and it can be concluded that device performance degradation due to fixed charges is more severe for device having larger dimensions (i.e. thicker silicon body, thicker insulating oxide, larger channel length). Analytical model developed in this work can thus be used to extract the density of localized charges present at the Si-SiO₂ interface of the GAA MOSFET. Developed model provides a simple approach to design equivalent circuit model for GAA MOSFET including hot carrier/stress/radiation damage induced fixed charges. The effect of hot
carrier damage/radiation damage/process damage induced localized charges has also been studied on the performance of the GAA MOSFET over a temperature range 100-500 K. Localized charges have a significant impact on the temperature sensitivity of the device which is harmful when the device is to be used in temperature sensitive environment. Since these localized charges are always present in a practical device, this study of estimation of performance degradation as a function of temperature is necessary so that device can be optimized accordingly. Having examined the impact of localized charges on the dc performance of GAA MOSFET, the next chapter emphasizes on impact of localized charges on analog RF/Microwave and linearity performance of the device.
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