Abstract

As silicon CMOS technology advances into the sub-50 nm regime, innovations in materials and device structures will be needed for further transistor miniaturization and enhanced device performance. Gate All Around (GAA) MOSFET is one of the most promising device architecture to extend the scaling of the CMOS device as it provides the best electrostatic control of the channel and nearly ideal subthreshold characteristics. Due to better gate control, GAA MOSFET is superior over Bulk MOSFET in terms of hot carrier reliability because of reduced short channel effects. The scaling trends in MOSFETs, operating conditions, process damage, and radiation damage give rise to serious device and circuit reliability issues. All these degradation mechanisms lead to generation of interface traps/localized charges at the Si-SiO$_2$ interface of the MOSFET. In nanoscale MOSFETs, the hot-carrier-induced degradation in form of interface traps, resulting from impact ionization in the channel near the drain junction, has become a major reliability concern as it results in reduced design margin for circuits. International Technology Roadmap for Semiconductors mentions reliability as one of the “Design Technology Challenges” and calls attention to “Design for Reliability”. With the increasing integration density of integrated circuits and reduction of dimensions of the device, even a small amount of interface traps/charges can have adverse effects on the device performance. In order to increase the overall design efficiency, it is important to (i) understand MOSFET-level degradation, (ii) develop analytical compact models including effects of interface charges and (iii) explore new device architectures/techniques which are self sufficient in preventing generation of interface traps. These interface localized charges change the device parameters such as threshold voltage, drain current, subthreshold slope, transconductance and cut-off frequency. In this dissertation, implications of hot carrier/stress/process/radiation damage induced interface localized charges on performance of Gate All around (GAA) MOSFET on device and circuit level are studied. An analytical model is developed for GAA MOSFET including interface localized charges. The model is able to predict the effect of density, extension and position of localized charges on the device performance degradation. Interface
charges not only affect the digital performance but also degrade the analog, RF/Microwave, linearity and circuit performance of the device. Therefore, complete study of localized charges degradation including analog, digital, RF/microwave, linearity and circuit performance of the device has been carried out through extensive device simulations. The analytical results are also compared with the simulated results using device simulator. Along with estimation of performance degradation, exploration of some techniques is required in order to address these reliability issues. In this research, GAA MOSFET with vacuum dielectric i.e. GAA VacuFET is proposed as a suitable replacement for the SiO$_2$ dielectric to have immunity against generation of hot carriers. The origin of all kinds of hot-carrier phenomenon is the large longitudinal electric field near the drain end of the channel. Therefore, the greatest control over hot-carrier effects is exerted by minimizing this longitudinal electric field. Electric field at the drain end is found to be much lower in case of vacuum dielectric as compared to SiO$_2$ dielectric. Also due to reduced gate to channel capacitance GAA MOSFET with vacuum dielectric shows superior RF performance over SiO$_2$ dielectric. But all these advantages are obtained at the cost of lower driving current capability. In this direction, Graded Channel Doping and Dual Material Gate engineering are combined with GAA VacuFET to enhance its driving current capability and transconductance without increasing the electric field at the drain junction. Just like dielectric in MOS devices influences the performance and reliability of the device, it also plays an important role when MOS devices are used in sensing applications. In this work, GAA MOSFET for various sensing applications has also been explored. GAA MOSFET with vacuum dielectric has been studied for biosensor and pH sensor applications based on dielectric modulation. GAA MOSFET with catalytic metal gate is studied for its use as a gas sensor. An analytical model is developed to model the response of GAA MOSFET in presence of external parameters such as pH change, dielectric constant and charges possessed by biomolecules etc. and analytical results are verified with device simulation results. GAA MOSFET shows much higher sensitivity for biosensing/pH sensing and gas sensing in subthreshold region as compared to conventional bulk MOSFET. High surface to volume ratio, low leakage current and
nearly ideal subthreshold slope (SS) makes GAA MOSFET a promising device architecture for developing a low power, highly sensitive, and nanoscale CMOS-compatible biosensor, pH sensor and gas sensor.