Chapter 5

Device Engineered Gate All Around (GAA) MOSFET for Improved Hot Carrier Reliability

5.1 Introduction

The scaling trends in MOSFETs, operating conditions, process damage and radiation damage give rise to serious device and circuit reliability issues. All these degradation mechanisms lead to generation of interface traps at the Si-SiO$_2$ interface of the MOSFET. It has been seen in the previous chapters that interface traps which can be effectively treated as equivalent localized/fixed charges at the Si-SiO$_2$ interface have a significant impact on the digital, analog, RF/Microwave and circuit performance of GAA MOSFET. Better fabrication techniques developed over the years, have managed to reduce the amount of interface traps. However, with increasing integration density of integrated circuits and reduction of device dimensions, even a small amount of traps can have adverse effects on the device performance. Thus, there is a need to explore some methods to address these issues of device and circuit reliability.

There are two ways to address these issues: the first method assumes that localized charges are already present in the device but their impact on the device performance can be subdued. The second method is about exploring a technique which can lead to reduction of electric field at the drain junction so that possibility of hot carrier generated interface states and thus localized charges is low. This chapter illustrates these two device engineering techniques to reduce the impact of localized charges and to reduce the hot carrier effect in the GAA MOSFET.
5.2 Gate Stack Engineering

The continued downscaling of CMOS technology in the nanoscale regime has also led to the requirement of ultra thin gate dielectrics. However, the thinning of oxide layer is limited by direct tunneling as it results in an increase in the leakage current thereby degrading the device reliability. In order to overcome this limitation, the focus was shifted to the use of high-$k$ dielectrics as alternative gate insulator materials to prevent tunneling. High-$k$ insulators can be grown physically thicker for the same (or thinner) Equivalent Oxide Thickness ($EOT$), thus offering significant reduction in electric field in the gate oxide, thereby, reducing gate leakage current, as demonstrated by several research groups [Momose96, Shimada96 and Wilk01]. But it degrades the device performance due to increased fringing fields from the source/drain regions which weakens the control of the gate over the channel [Yeap98]. Thus, an ultra thin SiO$_2$ interlayer between the high-$k$ layer and silicon substrate was introduced which also improves the interface quality and stability [Cheng99, Kauerauf05]. For stack gate dielectric structure, $t_{ox}$ is replaced with $t_{oxeff}$, where $t_{oxeff}$ is calculated adopting the effective oxide thickness formulation as:

$$t_{oxeff} = t_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} t_{ox2}$$  \hspace{1cm} (5.01)

Here, $t_{ox1}$ is the thickness of low-$k$ dielectric layer having permittivity $\varepsilon_{ox1}$ and $t_{ox2}$ is the thickness of high-$k$ dielectric layer having permittivity $\varepsilon_{ox2}$, constituting the stack architecture. Gate stack GAA MOSFET has already been demonstrated for suppression of DC performance degradation caused by hot carrier induced localized charges but it has been observed in this work that although gate stack architecture suppress the degradation due to localized charges but it also leads to higher parasitic capacitance and low cut-off frequency and is therefore, not suitable for RF/Microwave applications. Thus, asymmetric gate stack architecture is proposed in order to have immunity against degrading effects of localized charges on RF performance.
5.2.1 Asymmetric Gate Stack

In case of asymmetric gate stack, two-layer dielectric gate stack near the drain and single gate oxide near the source is used which is also advantageous in terms of reduced short channel effects and DIBL [Kaur07]. Fig. 5.01 (a) shows the schematic structure of asymmetric gate stack GAA MOSFET including localized charges. A step function distribution has been used for the density of localized charges. The length, location, type and density of localized charges have been defined using INTERFACE statement in ATLAS [Atlas10]. Simulation results are calibrated with the experimental results [Singh06] using (a) Lombardi CVT mobility model to consider parallel and perpendicular field dependence of mobility and mobility reduction effects due to various scattering mechanisms, (b) Energy Balance Transport (EBT) model to account for nonlocal transport effects such as velocity overshoot, (c) diffusion associated with the carrier temperature and the dependence of impact ionization rates on carrier energy distributions, (d) Bohr quantum potential model to take QMEs (Quantum Mechanical Effects) into consideration and (e) SRH recombination model to account for minority recombination. All these phenomena have a significant effect on the terminal properties of nanoscale devices as reported in [Roldán10]. Fig. 5.01 (b) shows the simulated results calibrated according to the experimental results [Singh06]. Amount of additional band bending taking place due to localized charges depends upon various parameters such as: density of localized charges ($N_f$), type of localized charges (positive or negative), thickness ($t_{ox}$) and dielectric permittivity ($\varepsilon_{ox}$) of the dielectric oxide layer and thickness of the silicon body ($t_{si}$) and is given by [Arora93]:

$$\Delta V_{fb} = \frac{qN_f}{C_{oxcy}cyl}$$ (5.02)

$C_{oxcy}$ is the gate oxide capacitance per unit area of the cylindrical-gate MOSFET, and is given as:

$$C_{oxcy} = \frac{2\varepsilon_{ox}}{t_{si} \ln \left(1 + \frac{2t_{ox}}{t_{si}}\right)}$$ (5.03)
Impact of symmetric and asymmetric gate stack on the performance degradation induced by localized charges is shown in Fig. 5.02. As can be seen from Fig. 5.02 (a), (b) and (c), a device with gate stack is more immune to degradation caused due to localized charges because of enhanced effective oxide capacitance and thus less change in the band
bending under the gate due to localized charges. Amount of change in band bending due to localized charges depends upon the oxide capacitance in accordance with eqn. (5.02) and gate stack results in enhanced $C_{ox}$ and thus less change in flat band voltage due to localized charges.

\[
\begin{align*}
\text{Figure. 5.02}\quad &\text{Impact of localized charges on } I_{ds}-V_{gs} \text{ characteristics of (a) GAA MOSFET, (b) Gate Stack GAA (GSGAA) MOSFET, (c) Asymmetric Gate Stack GAA (AGSGAA) MOSFET.} \\
&L=32 \text{ nm}, R=5 \text{ nm}, \\
&L_2=L/2, t_{ox}=3 \text{ nm}, t_{ox1}=t_{ox2}=1.5 \text{ nm}, N_d=1\times10^{26} \text{ m}^{-3}, N_a=1\times10^{21} \text{ m}^{-3}. \text{[Gautam13a]} \\
\end{align*}
\]

For GAA MOSFET without gate stack, $I_{off}$ is degraded by five (twelve) times for positive (negative) localized charges whereas with gate stack, $I_{off}$ is changed by only three (four) times. Similarly for asymmetric gate stack, only four (five) times degradation in $I_{off}$ is obtained for positive (negative) localized charges. Although gate stack leads to enhanced device gain as shown in Fig. 5.03 (a) but it also results in enhancement in gate to channel
capacitance as shown in Fig. 5.03 (b). Thus, gate stack degrades the device speed and cut-off frequency clearly as shown in Fig. 5.03 (c).

![Graphs](image)

**Figure. 5.03** (a) Tranconductance ($g_m$), (b) Gate to channel capacitance ($C_{gg}$), (c) Cut-off frequency ($f_T$) as a function of gate to source voltage ($V_{gs}$). L=32 nm, R=5 nm, $L_2=L/2$, $t_{ox}=3$ nm, $t_{ox1}=t_{ox2}=1.5$ nm, $N_d=1\times10^{26}$ m$^{-3}$, $N_s=1\times10^{21}$ m$^{-3}$. [Gautam13a]

Since localized charges are generally present near the drain side as drain is more prone to hot carrier or stress damage due to high electric field, thus, if gate stack is used only in half of the interface region (i.e. near the drain side where localized charges are present), it suppresses degradation caused due to localized charges similar to symmetric gate stack. Also degradation in cut-off frequency due to increased gate capacitance in asymmetric gate stack is also subdued as compared to symmetric gate stack. Performance of three
structures GAA MOSFET, Gate Stack GAA (GSGAA) MOSFET and Asymmetric Gate Stack GAA (AGSGAA) MOSFET is compared in Table 5.01.

**Table 5.01**

Impact of gate stack engineering on localized charge degradation. \(L=32\) nm, \(R=5\) nm, \(L_2=L/2\), \(t_{ox}=3\) nm, \(t_{ox1}=t_{ox2}=1.5\) nm, \(N_d=1\times10^{26}\) m\(^{-3}\), \(N_a=1\times10^{21}\) m\(^{-3}\). [Gautam13a]

<table>
<thead>
<tr>
<th>Without Gate Stack</th>
<th>With Symmetric Gate Stack</th>
<th>With Asymmetric Gate Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N_f=0)</td>
<td>(N_f=10^{16}) (m(^{-2}))</td>
<td>(N_f=-10^{16}) (m(^{-2}))</td>
</tr>
<tr>
<td>(I_{off}) ((\mu)A/(\mu)m) x 10(^3)</td>
<td>14</td>
<td>68</td>
</tr>
<tr>
<td>(I_{on}) ((\mu)A/(\mu)m)</td>
<td>101</td>
<td>103</td>
</tr>
<tr>
<td>(I_{on}/I_{off}) x 10(^3)</td>
<td>7.2</td>
<td>1.5</td>
</tr>
<tr>
<td>Peak (f_T) (GHz)</td>
<td>176</td>
<td>167</td>
</tr>
</tbody>
</table>

Symmetric gate stack results in enhancement in \(I_{on}/I_{off}\) by a factor of 2.5 for undamaged device because of effective gate control but at the same time, it also leads to 14% reduction in peak cut-off frequency due to larger gate to channel capacitance as shown in Fig. 5.03 (b). Now if instead of gate stack, asymmetric gate stack design is is used, a decent compromise between RF performance and immunity against degradation due to localized charges is achieved. The order of change in \(I_{on}/I_{off}\) due to positive (negative) localized charges is five (twelve), three (four), four (five) times for GAA MOSFET, GSGAA MOSFET and AGSGAA MOSFET respectively. Thus, asymmetric gate stack is also capable in suppressing degrading effects of localized charges. Also in case of asymmetric gate stack, peak cut-off frequency is only 7% lower than the device without gate stack. Thus, impact of localized charges can be suppressed using asymmetric gate stack along with better RF performance.
5.3 Vacuum Gate Dielectric

Hot carrier induced traps in the dielectric change device parameters such as threshold voltage, subthreshold slope, transconductance, and carrier mobility. Therefore, a comprehensive study of hot carrier reliability is necessary and it is also very important to explore a suitable replacement for the SiO$_2$ dielectric. FET with vacuum gate dielectric has been recently proposed [Han11] where vacuum gate dielectric is formed by a sacrificial layer deposition and removal process [Han11, Griesbach11] and is found to be resistant to hot carrier stress and radiation damage because of absence of solid material [Han11]. As far as fabrication of GAA VacuFET is concerned, well established and mature techniques (top-down and bottom-up) are already available in literature for fabrication of GAA MOSFET [Singh06] and VacuFET can be fabricated using sacrificial layer deposition and removal process [Han11, Griesbach11]. Vacuum gate dielectric is attained by complete removal of the SiO$_2$ sacrificial layer and measurement of the device under a vacuum ambient (<10$^{-6}$ Torr [Han11]). SiO$_2$ sacrificial layer is deposited using Chemical Vapor Deposition (CVD) method and for its removal hydrofluoric acid (HF) is used. The thickness of the vacuum gate dielectric is defined by the thickness of a sacrificial oxide layer which can be accurately controlled by matured CVD technology. Thus, fabrication of GAA VacuFET seems feasible in near future.

In vacuum gate dielectric, in contrast to SiO$_2$ gate dielectric, the impact ionization process driven by electrical bias has less probability to happen because of low electric field at the drain side and even if it persists it cannot damage the gate dielectric because the injected hot-carriers are collected by the gate electrode without charging or trapping in the dielectric. Therefore, the vacuum gate dielectric has the potential to provide a damage immune dielectric but it has a serious drawback of low current drivability as compared to SiO$_2$ dielectric due to lower gate to channel capacitance. As suggested in [Han11] the gate to channel capacitance can be improved by further reduction of the gate dielectric thickness but gate dielectric thickness cannot be scaled down beyond a certain limit, thus other means to enhance the current driving capability of GAA MOSFET with vacuum gate dielectric without increasing the electric field at the drain junction are to be
explored. Gate electrode engineering [Wei99, Chiang09] is one of the most sought out method to enhance the on current of the device but it also increases the off- current ($I_{\text{off}}$) at the same time thus leading to degradation in $I_{\text{on}}/I_{\text{off}}$ ratio. Another method is the channel doping engineering [Pavanello00, Kranti04] which decreases the off-current ($I_{\text{off}}$). Thus, by using both dual material gate and graded channel doping profile in GAA vacuFET, current driving capability can be enhanced without increasing the off current and electric field at the drain junction.

5.3.1 Analytical Model of GAA MOSFET with Vacuum Dielectric

To overcome the limitation of low drive current in vacuum dielectric, Dual Material Gate (DMG) and Graded Channel (GC) architectures are incorporated to enhance the driving current capability. This section presents an analytical model for DMG GC GAA MOSFET with vacuum gate dielectric and the simulation results of ATLAS 3-D device simulator [Atlas10] are used to validate the analytical results. Hot carrier reliability, dc and RF performance of the GAA MOSFET with vacuum gate dielectric is compared with GAA MOSFET with SiO$_2$ dielectric and other high-k dielectric materials.

5.3.1.1 Device Architecture

Fig. 5.04 shows the Schematic structure of DMG GC GAA MOSFET with vacuum gate dielectric. Table. 5.04 lists all the device parameters and their values which will be used in this model. To obtain analytic expression for potential distribution and drain current, channel region is divided into three regions as follows:

Region 1: $0 \leq z \leq L_1, 0 \leq r \leq R, N_A = N_{Ah}, \phi_m = \phi_{m1}$

Region 2: $L_1 \leq z \leq L_2, 0 \leq r \leq R, N_A = N_{Al}, \phi_m = \phi_{m1}$

Region 3: $L_2 \leq z \leq L, 0 \leq r \leq R, N_A = N_{Al}, \phi_m = \phi_{m2}$

Region 1 corresponds to highly doped region at the source side having gate metal workfunction $\phi_{m1}$, region 2 corresponds to lightly doped region at the middle having gate metal workfunction $\phi_{m1}$ and region 3 corresponds to lightly doped region at the drain side having gate metal workfunction $\phi_{m2}$. 
**Figure. 5.04**  Schematic structure of n-channel DMG GC GAA MOSFET with vacuum gate dielectric. \( L=100 \text{ nm}, R=10 \text{ nm}, N_{Ah}=5\times10^{23} \text{ m}^{-3}, N_{Al}=10^{21} \text{ m}^{-3}, N_{D}=10^{26} \text{ m}^{-3}, t_d=2 \text{ nm}, L_1=L_2=25 \text{ nm}, \Phi_{m_1}=4.58 \text{ eV}, \Phi_{m_2}=4.18 \text{ eV.} \) [Gautam13b]

**Table. 5.02**
List of parameters. [Gautam13b]

<table>
<thead>
<tr>
<th>Parameter symbol</th>
<th>Technology Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L )</td>
<td>Channel length</td>
<td>100nm</td>
</tr>
<tr>
<td>( R )</td>
<td>Channel Radius</td>
<td>10nm</td>
</tr>
<tr>
<td>( t_{si} )</td>
<td>Silicon film thickness=2R</td>
<td>20nm</td>
</tr>
<tr>
<td>( t_d )</td>
<td>Thickness of gate dielectric</td>
<td>2nm</td>
</tr>
<tr>
<td>( \phi_{m_1} )</td>
<td>Work function of Gate material 1</td>
<td>4.58eV</td>
</tr>
<tr>
<td>( \phi_{m_2} )</td>
<td>Work function of Gate material 2</td>
<td>4.18eV</td>
</tr>
<tr>
<td>( N_{Ah} )</td>
<td>Doping in the highly doped region near source side</td>
<td>( 5\times10^7 \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( N_{Al} )</td>
<td>Doping in the lightly doped region near drain side</td>
<td>( 10^{15} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( L_1 )</td>
<td>Length of region 1 having doping ( N_{Ah} ) and gate material ( M_1 )</td>
<td>25nm</td>
</tr>
<tr>
<td>( L_2 )</td>
<td>Length of region 2 having doping ( N_{Al} ) and gate material ( M_1 )</td>
<td>25nm</td>
</tr>
<tr>
<td>( L_3 )</td>
<td>Length of region 3 having doping ( N_{Al} ) and gate material ( M_2 )</td>
<td>50nm</td>
</tr>
</tbody>
</table>
5.3.1.2 Model Formulation

Since doping concentration and gate electrode work function is different in each region, potential distribution is obtained by solving the Poisson’s equation separately in each region as follows:

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial}{\partial r} \varphi_i(r,z) \right) + \frac{\partial^2}{\partial z^2} \varphi_i(r,z) = \frac{q N_A}{\varepsilon_{si}}
\]  \hspace{1cm} (5.04)

where \( i = 1, 2, 3 \) for region 1, 2 and 3 respectively.

\( \varphi_i(r,z) \) is the potential distribution in the silicon film, \( N_A \) is the doping in the silicon film, \( q \) is the electron charge and \( \varepsilon_{si} \) is the dielectric permittivity of silicon.

Using parabolic approximation [Chiang11] \( \varphi_i(r,z) \) is given by:

\[
\varphi_i(r,z) = P_{i0}(z) + P_{i1}(z)r + P_{i2}(z)r^2
\]  \hspace{1cm} (5.05)

Where \( P_{i0}(z), P_{i1}(z) \) and \( P_{i2}(z) \) are obtained by using boundary conditions given by:

1. The center potential is a function of \( z \) only:

\[
\varphi_i(r = 0, z) = \varphi_{ci}(z)
\]  \hspace{1cm} (5.06)

The electric field at the center of silicon film is zero:

\[
\left. \frac{d\varphi_i(r,z)}{dr} \right|_{r = 0} = 0
\]  \hspace{1cm} (5.07)

2. The electric field at the silicon oxide interface is given by:

\[
\left. \frac{d\varphi_i(r,z)}{dr} \right|_{r = R} = \frac{C_d}{\varepsilon_{si}} (V_{gs} - V_{fb} - \varphi_{si}(z))
\]  \hspace{1cm} (5.08)

\( V_{gs} \) is gate to source voltage and \( V_{fb} \) is the flat band voltage given by: \( V_{fb1} = V_{fb2} = \phi_{m1} - \phi_s \) and \( V_{fb3} = \phi_{m2} - \phi_s \). Here \( \phi_{m1} \) and \( \phi_{m2} \) is the work function of gate material 1 and 2 respectively and \( \phi_s \) is the work function of silicon.

\( C_d \) is the capacitance per unit area of the gate dielectric of the GAA MOSFET represented by:
\[ C_d = \frac{\varepsilon_d}{R \ln \left( 1 + \frac{t_d}{R} \right)} \] (5.09)

\( \phi_{ce}(z) \) is the potential at the center of the silicon film, \( \phi_{si}(z) \) is the surface potential, \( \varepsilon_d \) is the relative permittivity of gate dielectric layer, \( t_{si} \) is the silicon film thickness, \( R \) is the silicon pillar radius and \( t_d \) is the gate dielectric thickness. Using the above boundary conditions the potential in the silicon film is given by:

\[ \phi_i(r,z) = \phi_{si}(r,z) + \frac{C_d(V_{gs} - V_{fb} - \phi_{si}(r,z))}{2\varepsilon_{si}R} \left( r^2 - R^2 \right) \] (5.10)

Substituting back eqn. (5.10) in (5.04), a second order differential equation is obtained in terms of surface potential given by:

\[ \frac{d^2}{dz^2} \phi_{si}(z) - k^2 \phi_{si}(z) = -k^2 D_i \] (5.11)

Where \( k \) is given by:

\[ k^2 = \frac{2\varepsilon_d}{\varepsilon_{si}R^2 \ln \left( 1 + \frac{t_d}{R} \right)} = \frac{2C_d}{\varepsilon_{si}R} \] (5.12)

and \( D_i \) for various regions is given by:

\[ D_1 = V_{gs} - V_{fb1} - \frac{qN_A h}{\varepsilon_{si}k} \] (5.13)

\[ D_2 = V_{gs} - V_{fb2} - \frac{qN_A l}{\varepsilon_{si}k} \] (5.14)

\[ D_3 = V_{gs} - V_{fb3} - \frac{qN_A l}{\varepsilon_{si}k} \] (5.15)

Now solution of eqn. (5.11) is given by:

\[ \phi_{si}(z) = P_i e^{kz} + Q_i e^{-kz} + D_i \] (5.16)

Where coefficients \( P_i \) and \( Q_i \) are constants and are calculated using continuity equations of electric potential and field at the interface given by:
\[ \phi_{s1}(L_4) = \phi_{s2}(L_4) \]  \hspace{1cm} (5.17)

\[ \phi_{s1}(L_1+L_2) = \phi_{s2}(L_1+L_2) \]  \hspace{1cm} (5.18)

\[ \phi'_{s1}(L_1) = \phi'_{s2}(L_1) \]  \hspace{1cm} (5.19)

\[ \phi'_{s1}(L_1+L_2) = \phi'_{s2}(L_1+L_2) \]  \hspace{1cm} (5.20)

and the boundary conditions at the source and drain edges are

\[ \phi_{s1}(0) = V_{bi} \]  \hspace{1cm} (5.21)

\[ \phi_3(L) = V_{bi} + V_{ds} \]  \hspace{1cm} (5.22)

where \( V_{bi} \) is the built-in potential of the source/drain junction, \( V_{ds} \) is the drain to source voltage.

\[ P_1 = P_3 + \frac{1}{2} \left( \frac{D_2-D_3}{k^2} \right) \exp \left( -k(L_1+L_2) \right) + \frac{1}{2} \left( \frac{D_1-D_2}{k^2} \right) \exp \left( -kL_1 \right) \]  \hspace{1cm} (5.23)

\[ Q_1 = Q_3 + \frac{1}{2} \left( \frac{D_2-D_3}{k^2} \right) \exp \left( k(L_1+L_2) \right) + \frac{1}{2} \left( \frac{D_1-D_2}{k^2} \right) \exp \left( kL_1 \right) \]  \hspace{1cm} (5.24)

\[ P_2 = P_3 + \frac{1}{2} \left( \frac{D_2-D_3}{k^2} \right) \exp \left( -k(L_1+L_2) \right) \]  \hspace{1cm} (5.25)

\[ P_2 = P_3 + \frac{1}{2} \left( \frac{D_2-D_3}{k^2} \right) \exp \left( k(L_1+L_2) \right) \]  \hspace{1cm} (5.26)

\[ P_3 = \frac{1}{2 \sinh (kL)} \left[ \left( V_{bi} + V_{ds} \right) \left( D_3 \right) \right] - \left( V_{bi} + \left( \frac{D_1-D_2}{k^2} \right) \cosh(kL_1) - \left( \frac{D_2-D_3}{k^2} \right) \cosh(k(L_1+L_2)) \right) \exp(-kL) \]  \hspace{1cm} (5.27)

\[ Q_3 = \frac{1}{2 \sinh (kL)} \left[ \left( V_{bi} + \left( \frac{D_1-D_2}{k^2} \right) \cosh(kL_1) - \left( \frac{D_2-D_3}{k^2} \right) \cosh(k(L_1+L_2)) \right) \exp(-kL) \right] - \left( V_{bi} + V_{ds} + \frac{D_3}{k^2} \right) \]  \hspace{1cm} (5.28)

Drain current in subthreshold region is calculated using the 2-D potential (eqn. 5.10) and is given by:
Here \( n_i \) is the intrinsic carrier concentration and \( \mu \) is the carrier mobility. Threshold voltage \( (V_{th}) \) is calculated from the eqn (5.29) using constant current method \([Yan91, Lu05]\). The threshold voltage is measured at the drain current of \( 6 \times 10^{-7} \)A. For Linear region, drain current in region 1 i.e. \( I_{ds1} \) can be treated as a drain current of a GAA MOSFET with channel length \( L_1 \) and drain to source voltage equal to \( V_{p1} \). Similarly \( I_{ds2} \) can be treated as a drain current of a GAA MOSFET with channel length \( L_2 \) and drain to source voltage equal to \( (V_{p2} - V_{p1}) \) and \( I_{ds3} \) can be treated as a drain current of a GAA MOSFET with channel length \( L_1-L_1-L_2 \) and drain to source voltage equal to \( (V_{ds} - V_{p2}) \). Thus, it can be considered as three transistors having different properties connected in series. For linear region, current in each region is calculated separately and is given by:

\[
I_{ds1} = \frac{C_d \mu R}{L_1} \left( (V_{gs} - V_{th})V_{p1} - \frac{V_{p1}^2}{2} \right)
\]

\[
(5.30)
\]

\[
I_{ds2} = \frac{C_d \mu R}{L_2} \left( (V_{gs} - V_{th}) \left( V_{p2} - V_{p1} \right) - \frac{V_{p2}^2 - V_{p1}^2}{2} \right)
\]

\[
(5.31)
\]

\[
I_{ds3} = \frac{C_d \mu R}{L_3} \left( (V_{gs} - V_{th}) \left( V_{ds} - V_{p2} \right) - \frac{V_{ds}^2 - V_{p2}^2}{2} \right)
\]

\[
(5.32)
\]

Now to obtain unique value of drain current in the device, all three currents are equated to each other leading to two quadratic equation of the form given by:

\[
A_1 V_{p1}^2 + B_1 V_{p1} + C_1 = 0
\]

\[
(5.33)
\]

\[
A_2 V_{p2}^2 + B_2 V_{p2} + C_2 = 0
\]

\[
(5.34)
\]

Where \( A_1, A_2, B_1, B_2, C_1 \) and \( C_2 \) are given by:
\begin{align*}
A_1 &= -\frac{1}{2} \left( \frac{1}{L_4} + \frac{1}{L_2} \right) \\
B_1 &= \left( V_{gs} - V_{th} \right) \left( \frac{1}{L_4} + \frac{1}{L_2} \right) \\
C_1 &= \frac{V_{p2}^2}{2L_2} - \frac{\left( V_{gs} - V_{th} \right) V_{p2}}{L_2} \\
A_2 &= -\frac{1}{2} \left( \frac{1}{L_2} + \frac{1}{L_3} \right) \\
B_2 &= \left( V_{gs} - V_{th} \right) \left( \frac{1}{L_2} + \frac{1}{L_3} \right) \\
C_2 &= \frac{V_{p1}^2}{2L_2} + \frac{V_{ds}^2}{2L_3} - \frac{\left( V_{gs} - V_{th} \right) V_{p1}}{L_2} - \frac{\left( V_{gs} - V_{th} \right) V_{ds}}{L_3}
\end{align*}

Solution of quadratic equation gives the value of \( V_{p1} \) and \( V_{p2} \) which are then substituted back in any of the eqn. (5.30), (5.31) or (5.32) to obtain final drain current. Drain current in saturation region is calculated by replacing \( V_{ds} \) by saturation drain-to-source voltage \( (V_{dsat}) \) which is given by:

\[
V_{dsat} = \left( V_{gs} - V_{th} \right) \left( 1 + \frac{\left( V_{gs} - V_{th} \right) \mu}{L_{Vsat}} \right)
\]

where \( \mu \) is the low field mobility and \( v_{sat} \) is the saturation velocity for electron. Mobility reduction effects at higher electric field \([Jang98]\) are incorporated using:

\[
\mu_{fld} = \text{\textmu eff} \left( 1 + \delta \frac{V_{ds}}{V_{sat} L} \right) \text{ where } \text{\textmu eff} = \frac{\mu}{1 - \theta \left( V_{gs} - V_{th} \right)}
\]

\( \mu_{fld} \) is the field dependent mobility and \( \theta \) is a fitting constant whose value used in this work is \( \theta = 0.04 \) and

\[
\delta = \left( \frac{V_{ds} \mu}{L_{Vsat}} \right) \left( 1.5 + \frac{V_{ds} \mu}{L_{Vsat}} \right)^{-1}
\]

### 5.3.1.3 Model Validation and Calibration

ATLAS-3D device simulator \([Atlas10]\) has been used to simulate Si cylindrical GAA MOSFET with SiO\(_2\), dielectric, high-\( k \) dielectric and gate stack along with GAA
vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. Fig. 5.05 shows the 3-D schematic and 2-D simulated structures of DMG GC GAA MOSFET. Following models have been invoked during simulation.

1) **Carrier Transport Model**: Boltzmann transport model (drift diffusion approach) works quite well for channel length greater than 40 nm without compromising the accuracy of the simulated results [Granzner06].

2) **Mobility Model**: Low field mobility models: Carrier-Carrier Scattering Model (CCSMOB) and Surface degradation model (SURFMOB) with parameter ($\mu_{bn}=228$ cm$^2$/Vs i.e. bulk mobility) have been used to consider mobility reduction due to various scattering mechanisms such as: lattice scattering, impurity scattering and carrier-carrier scattering. On the other hand, for high field mobility reduction effects, parallel field dependent mobility model (FLDMOB) has been used in simulation with parameters ($\nu_{sat}=1.03\times10^7$ cm/s, $\beta=2$).

![Figure 5.05](image)

**Figure. 5.05** (a) 3D-schematic of the n-channel GAA-MOSFETs structure. (b) Numerical simulation structure used to validate the analytical model. $L=100$ nm, $R=10$ nm, $N_{\text{Al}}=5\times10^{23}$ m$^{-3}$, $N_{\text{Ah}}=10^{21}$ m$^{-3}$, $\Phi_{m1}=4.58$ eV, $\Phi_{m2}=4.18$ eV. [Gautam13b]
3) **Generation Model**: Hot electron injection model is invoked to calculate hot electron injected gate current in the device.

4) **Recombination Model**: Shockley-Read-Hall recombination model (with carrier lifetime $1\times10^7$ s) is included in simulation to incorporate minority recombination effects.

5) **Quantum Model**: Quantum Mechanical effects (QMEs) plays as important role in the electrical characteristics of GAA MOSFET when the silicon pillar radius is less than 5 nm [Tsormpatzoglou09], however in present work QMEs are not taken into account because substrate doping ($N_A$) is $10^{15}$ cm$^{-3}$ (i.e. undoped case) and channel (silicon pillar) radius is 10 nm.

Calibration of model parameters used in simulation has been performed according to the experimental results [Hong11]. Fig. 5.06 shows the simulated doping profile along the length from source to drain. Closed proximity of simulated results with the experimental results as shown in inset of Fig. 5.06 validates the choice of parameters taken in modeling and simulation.

![Simulated doping profile](image)

**Figure. 5.06**  Simulated doping profile along the length from source to drain. $L=100$ nm, $R=10$ nm, $N_{A0}=5\times10^{21}$ m$^{-3}$, $N_{A1}=10^{21}$ m$^{-3}$, $N_D=10^{26}$ m$^{-3}$, $t_d=2$ nm, $L_1=L_2=25$ nm, $\Phi_{m1}=4.58$ eV, $\Phi_{m2}=4.18$ eV. Inset: calibration with experimental results [Hong11], $L=300$ nm, $R=5$ nm, $t_d=3.5$ nm. Symbol: experimental, Line: simulated. [Gautam13b]
5.3.2 Comparison of Vacuum Dielectric with SiO$_2$ and High-$k$ dielectrics

Hot carrier reliability can be judged upon by the electric field and electron temperature profile in the channel and hot electron injected gate current [Ren02, Naseh06]. Fig. 5.07 illustrates the surface electric field for GAA MOSFET with SiO$_2$ dielectric and vacuum dielectric.

Both the devices are optimized for the same threshold voltage. It clearly shows that electric field at the drain junction is much lower (30%) for vacuum dielectric as compared to SiO$_2$ dielectric. Thus, there is a less probability of generation of hot carriers in GAA MOSFET with vacuum dielectric as compared to SiO$_2$ dielectric. Energy Balance Model (with Energy relaxation time of 0.4 ps) was invoked in simulation to calculate electron temperature in order to assess the hot carrier reliability of the device. Fig. 5.08 shows the electron temperature in the channel for $V_{gs}=1$ V and $V_{ds}=1$ V. The temperature at the drain end is 1297 K for SiO$_2$ dielectric whereas 711 K for vacuum dielectric. Thus, at the drain junction, electron temperature is nearly two times lower for vacuum dielectric than SiO$_2$ dielectric. Thus, it shows that probability of hot carrier generation is low in vacuum gate dielectric case.
Fig. 5.08  Electron temperature [Simulated] as a function of position along the channel. L=100 nm, R=10 nm, $N_A=10^{21}$ m$^{-3}$, $N_D=10^{26}$ m$^{-3}$, $t_d=2$ nm. [Gautam13b]

Fig. 5.09 illustrates the hot electron injected gate current comparison between SiO$_2$ dielectric and vacuum dielectric. As can be seen low gate current is obtained in case of vacuum dielectric and even if hot carrier generation/impact ionization takes place, it cannot damage the vacuum gate dielectric because the injected hot-carriers are collected by the gate electrode without charging or trapping in the gate dielectric (as it is vacuum) [Han11]. Thus, vacuum dielectric has better hot carrier reliability.

Fig. 5.09  Hot electron injected gate current [Simulated] as a function of drain to source voltage. L=100 nm, R=10 nm, $N_A=10^{21}$ m$^{-3}$, $N_D=10^{26}$ m$^{-3}$, $t_d=2$ nm. [Gautam13b]
But immunity from the degrading effects of fixed charges is obtained at the cost of low drive current due to low gate to channel capacitance as shown in Fig. 5.10. The value of on current ($I_{ds} @ V_{gs}=1 \text{ V}, V_{ds}=1.0 \text{ V}$ [Iwai09]) is ~ 4 times smaller for GAA MOSFET with vacuum dielectric as compared with SiO$_2$ dielectric which also affects the device gain as shown in Fig. 5.11 (a) where peak transconductance is 4 times less for vacuum dielectric. On the other hand, for RF applications, GAA MOSFET with vacuum gate dielectric (GAA vacuFET) is a promising candidate as shown in Fig. 5.11 (b) which shows the gate to source capacitance ($C_{gs}$) comparison for both the devices. As shown in Fig. 5.11 (b), GAA vacuFET has four times lower $C_{gs}$ (at $V_{gs}=1 \text{ V}, V_{ds}=1 \text{ V}$) than SiO$_2$ dielectric thus suitable for high speed applications. Cut off frequency is determined from $C_{gs}$ as well as from $g_{m}$, therefore, peak cut-off frequency for vacuum dielectric is higher than SiO$_2$ dielectric due to much lower $C_{gs}$ in vacuum case. Thus, GAA MOSFET with vacuum dielectric outperforms GAA MOSFET with SiO$_2$ dielectric for high speed RF applications along with advantages of immunity against hot carrier/radiation damages.

Figure. 5.10  Drain current as a function of gate to source voltage for GAA MOSFET with SiO$_2$ and vacuum dielectric. Dashed line: SiO$_2$, solid line: Vacuum. $L=100 \text{ nm}, R=10 \text{ nm}, N_A=10^{21} \text{ m}^{-3}, N_D=10^{26} \text{ m}^{-3}$, $t_d=2 \text{ nm}, V_{ds}=1 \text{ V}$. [Gautam13b]
Thus, there is a need to explore methods in order to enhance current driving capability of GAA vacuFET without increasing the electric field at the drain junction. Dual Material Gate (DMG) is one method to increase the on-current without increasing the electric field at the drain junction as shown in Fig. 5.12 (a). DMG GAA vacuFET leads to additional peak at the interface of two metal gates which increases the average carrier velocity leading to increase in on-current whereas field at the drain junction is lowered leading to further less probability of hot carrier generation but DMG increases the off leakage current at the same time. On the other hand, graded channel doping lowers the off-current. Thus, if DMG is combined with graded channel doping then higher drive current is obtained along with a good $I_{on}/I_{off}$ ratio. Fig. 5.12 (b) shows the surface potential for GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. Close proximity of the analytical results with the simulated results validates the analytical model. Fig. 5.13 shows $I_{ds}-V_{gs}$ characteristics where improvement in on current is visible when DMG and GC are used with GAA MOSFET with vacuum dielectric.
Figure 5.12  (a) Surface electric field  (b) Surface potential as a function of position along the channel for GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. L=100 nm, R=10 nm, t_d=2 nm, V_{ds}=1 V. [Gautam13b]

Figure 5.13  Drain current as a function of gate to source voltage for GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. L=100 nm, R=10 nm, t_d=2 nm, V_{ds}=1 V. [Gautam13b]

Fig. 5.14 (a) shows the comparison of the three structures for transconductance. It clearly shows that DMG GC leads to 25% improvement in peak g_m. Fig. 5.14 (b) illustrates that not only higher value of (a) drive current, (b) I_{on}/I_{off}, (c) device gain and (d) hot carrier immunity is obtained for DMG GC GAA vacuFET but gate-to-source capacitance (C_{gs}) is also improved leading to higher device speed of operation. Fig. 5.14 (c) demonstrates the cut-off frequency (f_T) for the four devices and it shows that DMG GC GAA vacuFET has the highest peak f_T.
Figure 5.14 (a) Transconducance (b) Gate to source capacitance (c) Cut-off frequency as a function of gate to source voltage for GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. [Simulated]. L=100 nm, R=10 nm, t_d=2 nm, V_{ds}=1 V. [Gautam13b]

Another important parameter to investigate analog performance is device efficiency (g_m/I_{ds}). Higher g_m/I_{ds} value indicates higher transconductance and thus stronger capability to convert dc power into ac gain at a certain drain bias. Fig. 5.15 illustrates comparison of g_m/I_{ds} for GAA with SiO_2 dielectric, GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. It shows that efficiency in VacuFET is comparable to SiO_2 case.
Figure. 5.15 \( \frac{g_m}{I_{ds}} \) as a function of gate to source voltage for GAA MOSFET with SiO\(_2\) dielectric, GAA vacuFET, DMG GAA vacuFET and DMG GC GAA vacuFET. [Simulated]. \( L=100 \text{ nm}, R=10 \text{ nm}, N_A=10^{21} \text{ m}^{-3}, N_D=10^{26} \text{ m}^{-3}, t_g=2 \text{ nm}, V_{ds}=1 \text{ V}. \) [Gautam13b]

Table. 5.03 illustrates the comparison of overall performance of GAA with vacuum as dielectric, with SiO\(_2\) dielectric, high-\( k\) dielectric and high-\( k\) gate stack. As can be seen from Table. 5.03, very low value of off current \( (I_{off}) \) is obtained for GAA MOSFET because of its effective gate control and better subthreshold characteristics [Jiménez04, Abdi11]. RF performance of various architectures is compared in two ways i.e. one is comparison of peak/maximum values of cut-off frequency \( (f_{tmax}) \) and gate-to-source capacitance \( (C_{gssmax}) \) and other method is comparing their values at typical operating bias points i.e. \( V_{gs}-V_{th}=0.5 \text{ V}, V_{ds}=1 \text{ V} \) [Lazaro06, Nae11]. As can be seen from Table. 5.03, DMG GC GAA vacuFET has highest cut-off frequency among all architectures along with decent analog performance, better carrier transport characteristics and immunity against hot carrier degradation. Thus, DMG GC GAA vacuFET outperforms over its conventional counterparts (SiO\(_2\) dielectric, high-\( k\) dielectrics and high-\( k\) gate stack) for RF applications and also provides better immunity against hot carrier degradation.
Table 5.03
Performance comparison for various architectures based on numerical simulations. L=100 nm, R=10 nm, \( t_d=2 \) nm, \( V_{ds}=1 \) V. [Gautam13b]

<table>
<thead>
<tr>
<th></th>
<th>GAA SiO(_2) dielectric</th>
<th>GAA High-( k ) dielectric ( k=22 )</th>
<th>GAA High-( k ) gate stack ( k=22 )</th>
<th>GAA Vacu-FET</th>
<th>DMG GAA Vacu-FET</th>
<th>DMG GC GAA Vacu-FET</th>
<th>DMG GC GAA SiO(_2) dielectric</th>
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<tbody>
<tr>
<td>( I_{on} (\mu A) )</td>
<td>40.2</td>
<td>163</td>
<td>97.6</td>
<td>10.8</td>
<td>14</td>
<td>12.7</td>
<td>51.7</td>
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<tr>
<td>( I_{off} (pA) )</td>
<td>45.7</td>
<td>34.9</td>
<td>40.2</td>
<td>6.35</td>
<td>79.3</td>
<td>14.4</td>
<td>88.9</td>
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<tr>
<td>( I_{on}/I_{off} \times 10^5 )</td>
<td>8.8</td>
<td>46.6</td>
<td>14.9</td>
<td>17</td>
<td>1.76</td>
<td>8.78</td>
<td>5.8</td>
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<tr>
<td>( g_{mmax}@V_{gs}=1V )</td>
<td>0.078</td>
<td>0.336</td>
<td>0.122</td>
<td>0.021</td>
<td>0.024</td>
<td>0.024</td>
<td>0.09</td>
</tr>
<tr>
<td>( g_m@V_{gs}=V_{th}=0.5V ) (mS)</td>
<td>0.069</td>
<td>0.302</td>
<td>0.109</td>
<td>0.019</td>
<td>0.022</td>
<td>0.0528</td>
<td>0.085</td>
</tr>
<tr>
<td>( C_{gsmax}@V_{gs}=1V )</td>
<td>89.6</td>
<td>419</td>
<td>143</td>
<td>22.4</td>
<td>22.9</td>
<td>22.5</td>
<td>92.6</td>
</tr>
<tr>
<td>( C_{gs}@V_{gs}=V_{th}=0.5V ) (aF)</td>
<td>84.9</td>
<td>414</td>
<td>136</td>
<td>21.1</td>
<td>22.0</td>
<td>21.5</td>
<td>89.7</td>
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<tr>
<td>( f_{Tmax}@V_{gs}=1V )</td>
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<td>122</td>
<td>127</td>
<td>130</td>
<td>141</td>
<td>143</td>
<td>140</td>
</tr>
<tr>
<td>( f_{T}@V_{gs}=V_{th}=0.5V ) (GHz)</td>
<td>120</td>
<td>112</td>
<td>119</td>
<td>124</td>
<td>139</td>
<td>141</td>
<td>136</td>
</tr>
<tr>
<td>( g_{m}/I_{ds} ) (V(^{-1}))</td>
<td>38.2</td>
<td>39</td>
<td>39.8</td>
<td>37.2</td>
<td>34</td>
<td>34</td>
<td>38.4</td>
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</table>

5.4 Summary

Two device architectures i.e. asymmetric gate stack GAA MOSFET and GAA MOSFET with vacuum dielectric are discussed in this chapter to improve the hot carrier reliability of the device. Although gate stack architecture suppresses the degradation caused by localized charges but due to higher dielectric constant, it also leads to higher parasitic capacitance and low cut-off frequency and is therefore, not suitable for RF applications. Since hot carrier induced charges are generally located near the drain side, asymmetric gate stack design is proposed for suppression of degradation due to localized charges along with improved RF performance. Another structure for improved hot carrier
reliability is GAA MOSFET with vacuum dielectric. Apart from hot carrier reliability, GAA MOSFET with vacuum dielectric shows better performance than GAA MOSFET with SiO₂ dielectric for high speed and RF applications but suffers from a serious drawback of lower drive current. Thus, Dual Material Gate and Graded Channel Doping are incorporated to enhance the drive current and transconductance of GAA VacuFET without increasing the I_{off} and electric field at the drain junction. DMG GC architecture not only improves the analog performance but the RF performance is also improved along with lower electric field at the drain junction which further improves hot carrier reliability. DMG GC GAA VacuFET with vacuum dielectric is found to have higher cut-off frequency as compared to its SiO₂ counterpart and other high-\( k \) dielectrics, thus, most suitable candidate for high speed RF applications along with better hot carrier reliability. Due to effective gate control and high surface to volume ratio, GAA MOSFET is also a suitable candidate for sensor applications. The next chapter covers this topic and explores the capabilities of GAA MOSFET for various sensing applications such as biosensor, pH sensor and gas sensor.
5.5 References


Chapter 5: Device Engineered Gate All Around...


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