Modeling, Simulation and Characterization of Noise in InAlAs/InGaAs Tied-geometry Double-gate High Electron Mobility Transistor for Millimeter-wave Applications

By

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ABSTRACT

I do not think there is any thrill that can go through the human heart like that felt by the inventor as he sees some creation of the brain unfolding to success... such emotions make a man forget food, sleep, friends, love, everything.

Nikola Tesla

Every development in science and technology is envisioned with a primary motive of serving the society with its ever growing demands. The invention of bipolar junction transistor that took place in the mid of the 20th century is considered as one of the greatest inventions of mankind that also marked the emergence of integrated circuit technology. Unprecedented growth in solid state transistors and integrated circuit technology has taken place over the past sixty years. The sole aim has been to produce transistors that are smaller, faster, consume less power, are cheaper to manufacture and enable large packing densities. Underlying this breathtaking electronics revolution has been a remarkable evolutionary trend called Moore’s Law which began as a simple observation that the number of components integrated into a semiconductor circuit doubled each year for the first few years of the industry and eventually came to represent the amazing and seemingly inexhaustible capacity for exponential growth in electronics. Considerable reduction in the size of silicon based
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transistors has already taken place from a few tens of micron length channel to sub 25 nm length channel. Downscaling of silicon based transistor has almost reached its saturation limit and consequently, Moore’s Law is sometimes believed to be in a very real danger of losing its meaning, and possibly its usefulness. Fortunately, introduction of innovative gate architectures and improvement in fabrication techniques has kept alive, the pace of development in Si VLSI technology. Due to continuous advancement, integrated circuits with complexities of over tens of millions of transistors on a single chip that seemed imaginable about a few decades ago have become a reality.

Besides, the Si VLSI technology, which has been by far the most dominant technology for digital applications such as in microprocessors and semiconductor memories, another class of transistor technology that has undergone tremendous advancement and has received a lot of attention over the past three decades is that of “radio-frequency” or RF transistors. Transistors capable of operating in gigahertz frequency range are essentially referred to as radio frequency transistors. Germanium based bipolar junction transistors which emerged in late 1950s were the first transistors that found capable of producing amplification upto 1 GHz. They were soon replaced by Silicon BJTs which were found to be more stable at higher temperatures and exhibited a much higher frequency of operation upto 35 GHz. The major drawback of Si based RF transistors is the inherent low electron mobility of Silicon which puts a limitation on its high speed performance. Compound semiconductor material such as Gallium Arsenide having much higher electron mobility than Silicon was found to be more appropriate for the implementation of high speed transistors. GaAs based Metal Semiconductor Field Effect Transistors introduced in the late 1960s produced maximum frequency of oscillation exceeding 100 GHz which was much higher than that obtained for Silicon BJTs. Till 1980, Si BJTs and GaAs MESFET were the only two RF transistor technologies available. In GaAs MESFET, the channel is formed in the doped layer itself which results in significant degradation in the carrier mobility on account of ionized impurity scattering. This posed a fundamental limitation on the maximum performance improvement that can be obtained with MESFET. This initiated yet another quest for alternative transistor
technology in which the superior carrier mobility obtained in a compound semiconductor material can be preserved and fully exploited.

The emergence of high electron mobility transistor, HEMT which was first experimentally demonstrated by Takashi Mimura of Fujitsu Laboratories in 1981 can be regarded as another major milestone in this regard that took the frequency of operation and noise handling capability of solid state transistors to a new level. Over the past three decades, tremendous advancement in HEMT technology has taken place. Since the first generation lattice matched AlGaAs/GaAs high electron mobility transistors, a large number of material systems have been explored for the fabrication of HEMT. Amongst the various types of HEMTs which are available today, AlGaAs/InGaAs/GaAs Pseudomorphic HEMT and InAlAs/InGaAs/InP lattice matched and Pseudomorphic HEMT have been of greatest interest with respect to ultra-high speed applications.

HEMT technology has undergone tremendous advancement. Through aggressive device scaling along with improvement in the fabrication techniques, the frequency of operation and noise performance of high electron mobility transistors have touched amazingly new heights which is incomparable to any other transistor technology available today. InP based InAlAs/InGaAs HEMTs have particularly exhibited excellent performance with a high current-gain cut-off frequency of 562 GHz and a high maximum frequency of oscillation of 330 GHz reported for a 25 nm gate-length device which have made them the most desirable for ultra-high speed applications. Further improvement in device performance calls for further reduction in gate-length. Gate-length reduction, however, also has a certain limit beyond which the various short channel effects which include the threshold voltage shift, reduced transconductance and increased output conductance become dominant which cause degradation in the device performance. This implies that beyond the limit of device miniaturization, improvement in the device performance cannot be achieved just through reduction in gate-length and alternative techniques are required. One such technique is to employ modified gate-structures such as the double-gate structure. In a double-gate structure, two gates are placed on both sides of the channel which leads to
better control of the gate voltage over the conducting channel which in turn results in improvement in transconductance.

InAlAs/InGaAs double-gate HEMT recently fabricated using the transferred substrate technique has exhibited excellent microwave and noise performance as compared to its single-gate counterpart in terms of lower Minimum Noise Figure and higher Maximum Frequency of oscillation. This has generated great interest in the device and a comprehensive analytical device model is now desirable for microwave and noise performance characterization of the device. The present work is focussed on modeling and simulation of InAlAs/InGaAs double-gate high electron mobility transistor for the assessment of its noise performance at millimeter-wave frequencies.

In Chapter 1, a brief insight into how the radio frequency transistor technology has evolved from early Silicon based bipolar junction transistors to present day high electron mobility transistors is provided. The microwave and noise performance of various III-V HEMT technologies which are available today are also compared which establishes InP based InAlAs/InGaAs lattice matched and pseudomorphic HEMTs as the most suitable choice for low noise millimeter-wave frequency applications. Then, the major reasons responsible for the inevitable switching from the conventional single-gate structure to double-gate structure are discussed. Motivated by the excellent microwave and noise performance experimentally reported for InAlAs/InGaAs double-gate HEMT as compared to its single-gate counterpart, the work presented in the subsequent chapters aims at development of a comprehensive analytical model for InAlAs/InGaAs double-gate for the assessment of its noise performance at ultra-high frequencies.

In Chapter 2, a small-signal equivalent circuit model for lattice matched tied-geometry InAlAs/InGaAs double-gate HEMT is formulated. Drain current and the various equivalent circuit parameters including transconductance, drainconductance and gate-capacitances are thereby obtained from the proposed model. The current-gain cut-off frequency which is a major performance parameter governing the high speed performance of the device is also then evaluated in terms of the transconductance and gate-capacitances. Double-gate HEMT is found to exhibit better performance single-gate HEMT in terms of higher drain current and improved
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transconductance. The analytically obtained transfer characteristics, i.e., drain-current vs gate voltage characteristics are found to agree reasonably well with the experimental measurements, thereby, proving the validity of the proposed model. Due to higher sheet carrier concentration in the channel of a double-gate HEMT, its performance in terms of drain current and transconductance is more sensitive to various device parameters including donor layer doping, donor-layer thickness, gate-length and channel width. Therefore, the effect of these device parameters on the drain current and small signal equivalent circuit parameters of InAlAs/InGaAs DG-HEMT as compared to the SG-HEMT is also studied. Chapter 3 deals with the evaluation of the scattering parameters of InAlAs/InGaAs double-gate HEMT employing the charge control model proposed in the previous chapter. With respect to application of device in microwave active circuits, the knowledge of its scattering parameters is inevitable. It is in terms of these scattering parameters, the various RF performance parameters including Maximum Unilateral Power Gain, Maximum Stable Gain and the Maximum frequency of Oscillation are obtained. The scattering parameters and the power gains obtained using the proposed model is also validated with the device simulation results.

In addition to the high speed performance of the device, the assessment of its noise performance is also important. In Chapter 4, a comprehensive charge control based modeling approach based on Pucel’s PRC noise theory is followed for the noise performance assessment of InAlAs/InGaAs double-gate and single-gate HEMT. The dependence of fermi-potential $E_f$ with the sheet carrier concentration $n_s$ is approximated using a quadratic polynomial. Drain current and the various small-signal equivalent circuit elements are thereby obtained which is followed by the evaluation of the intrinsic noise sources, i.e., gate noise current source at the input and drain noise current source at the output. The major figures of merit of noise performance including the noise resistance and the Minimum Noise Figure are then obtained. DG-HEMT is observed to exhibit better noise performance as compared to its single-gate counterpart in terms of reduced Minimum Noise Figure. The analytical results obtained are compared and found to agree reasonably well with the ATLAS device simulation results as well as with experimental and Monte-Carlo simulation
data reported elsewhere. The dependence of gate-drain capacitance ($C_{gd}$) has also been incorporated in the model for a more accurate evaluation of Minimum Noise Figure and other performance parameters at low drain voltage at which the magnitude of $C_{gd}$ is very high. The proposed charge control based model for symmetric tied-gate geometry InAlAs/InGaAs double-gate (DG) HEMT enables a comprehensive noise performance assessment of the device. In Chapter 5, the charge control based analytical model proposed in the previous chapter is extended to incorporate the impact of temperature on various microwave and noise performance parameters of the device. A more comprehensive analysis is thereby carried out over a broad temperature range extending from -50 °C to 200 °C which is important for establishing device reliability in various practical applications. Moreover, the effect of indium mole-fraction, $m$ in the In$_m$Ga$_{1-m}$As channel on the device performance is also studied. Chapter 6 finally summarises the work presented in the thesis with the major conclusions drawn from the results obtained. The scope of present work for future research is also highlighted.
List of Publications

- **Publications in Referred/Peer Reviewed International Journals**


  (iii) **Monika Bhattacharya**, Jyotika Jogi, R.S Gupta and Mridula Gupta, “Temperature Dependent Analytical Model for Microwave and Noise Performance Characterization of In$_{0.52}$Al$_{0.48}$As/In$_m$Ga$_{1-m}$As (0.53 ≤ m ≤ 0.8) DG - HEMT”, *IEEE Transactions on Device and Material Reliability*, Vol.13, No.1, pp.293-300, (March) 2013. **Impact Factor (2013): 1.543**.


  (v) **Monika Bhattacharya**, Jyotika Jogi, R.S. Gupta and Mridula Gupta, “Temperature and Channel Indium Composition Sensitivity Analysis of the Small-Signal Equivalent Circuit Parameters of SG- and DG- InAlAs/InGaAs HEMT”, *Conditionally Accepted for publication in IEEE Transactions on Nanotechnology*, 2013.

- **Publications in International Conference Proceedings**


  (ii) **Monika Bhattacharya**, Jyotika Jogi, R.S. Gupta and Mridula Gupta, “Temperature and Channel Indium Composition Sensitivity Analysis of the Small-Signal Equivalent Circuit Parameters of SG- and DG- InAlAs/InGaAs HEMT”, *Proceedings of NANOCON 2012 (2nd International Conference on*


- **Publications in National Conference Proceedings**

(xi) **Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta**, “Gate-length and Donor-layer characteristics Optimization of InAlAs/InGaAs DG-HEMT for improved RF and Noise Performance”, *Proceedings of NCRDE-2013 (National Conference on Recent Developments in Electronics)*, Department of Electronic Science, University of Delhi, South Campus, January 18-20, 2013.