CHAPTER 6

Analysis of Empty Space in Double Gate (ESDG) Architecture: A Novel Device Design
6.1 Introduction

The rigorous scaling of CMOS technology has made it attractive for System-On-Chip (SOC) applications, where the analog circuits are realized along with digital circuits in the same integrated chip to reduce cost and to improve the performance of the circuit. In nano-scale devices, undesirable Short channel Effects (SCEs) and leakage current are also major source of concern that adversely affect the performance of the circuit. To relieve these problems, many non-conventional CMOS devices were proposed to suppress the SCEs [Hutchby02] [Burghartz13]. To cope up with the scaling issues of nano-scale devices, various multiple gate structures with two gate on two or more sides of the channel have also been suggested and successfully realized [Schwierz10]. Planar Double Gate (DG) MOSFET [Balestra87] can also be considered as a extension of single gate Silicon On Insulator (SOI) MOSFET [Coling02] [Balamurugan09] [Liu10] to which a back gate is added [Schwierz10]. Lateral channel engineering technique in which dielectric pockets (or insulating layers) are placed inside the source/drain S/D regions are also reported to suppress drain side electric field and hence leakage current [Jurczak01]. In 1999, Sato et al. [Sato99] presented a new device design in which empty space layer or insulating layer (i.e. substrate engineering technique) is present in between the channel region i.e. Empty Space in Silicon (ESS) MOSFET as shown in figure 6.01 (also known as Silicon On Nothing/Void (SON/SOV) MOSFET [Allibert01] [Tian05]). ESS MOSFET suppress the undesirable coupling between S/D regions and drain substrate region and hence leakage current [Monfray01].

![Figure 6.01 Schematic cross section view of the Empty Space in Silicon (ESS) MOSFET.](image-url)
In last chapter, the performance of the DG MOSFET is further enhanced by using Dielectric Pockets (or insulating layers) at the side walls of the channel region known as Double Gate MOSFET incorporating Dielectric Pocket (DP-DG) MOSFET. DP-DG MOSFET suppresses the electrostatic coupling between drain and source region and thereby showing reduction in various parasitic capacitances associated with the DG MOSFET (i.e. gate to source capacitance $C_{gs}$ and gate to drain capacitance $C_{gd}$). Inspite of the various advantages offered by DP-DG MOSFET in comparison to DG MOSFET, it also suffers from some drawbacks such as reduction in on-state current ($I_{on}$) as well as in trans-conductance ($g_m$).

In this chapter, the parasitic capacitances associated with the conventional DG MOSFET is suppressed by introducing buried dielectric (Air) or empty space layer in between the channel region of Double Gate MOSFET resulting in a new device called as Empty Space in Double Gate (ESDG) MOSFET [Kumari11] [Kumari12] and is shown in figure 6.02.

The potential advantages of ESDG MOSFET as compared to DG and Bulk MOSFET are: 1) high on-state current ($I_{on}$), 2) nearly ideal sub-threshold slope ($S$), 3) reduction in Short Channel Effects (SCEs), 4) suppression of various parasitic capacitances and 5) immunity against random dopant fluctuation resulting in higher carrier mobility.

**Figure 6.02** Three dimensional view of the Empty Space in Double Gate (ESDG) MOSFET: $t_{ox}$ and $t_{box}$ are the thickness of the gate oxide region and empty space region respectively [Kumari13b].
Thus, in this chapter ESDG MOSFET has been examined analytically by calculating two dimensional electrostatic potential in the channel region using Evanescent Mode Analysis (EMA) [Lee04] which is further used to obtain drain current ($I_{ds}$), threshold voltage ($V_{th}$) and sub-threshold slope ($S$). The analytical results are verified with the ATLAS 3D device simulator [ATLAS10]. The impact of length of empty space layer on the performance of ESDG MOSFET has also been examined by investigating various parameters like threshold voltage ($V_{th}$), sub-threshold slope ($S$) and Drain Induced Barrier Lowering (DIBL) effect. The performance of the ESDG MOSFET for analog and digital applications have also been investigated through exhaustive device simulation and are compared with the conventional ESS and DG MOSFETs.

All the aforementioned parameters are studied with the help of a 3D device simulation and mixed mode circuit simulation [ATLAS10], and a comparison is made between the devices optimized to have the same threshold voltage (i.e. 0.25 V at $V_{ds}=0.5$ V) by changing the metal gate work-function of the devices.

The rest of the parameters of the devices are kept constant i.e., channel length ($L$), channel thickness ($t_{si}$), empty space layer thickness and gate oxide thickness.

### 6.2 Fabrication Feasibility of ESDG MOSFET

Till date the fabrication of proposed ESDG MOSFET was not discussed in the literature. However, various fabrication techniques for conventional ESS MOSFET (also known as silicon On Nothing MOSFET) and Double Gate MOSFET have been reported in the literature.

In 2001, Sato et al. proposed the fabrication feasibility of Empty Space in Silicon (ESS) MOSFET having 250 nm channel length [Sato01]. Further, various techniques to fabricate the conventional SON MOSFET have already been reported in literature and are also discussed in chapter 2.

In 2003, Harrison et al. demonstrated the fabrication feasibility of SON DG MOSFET for 45 nm gate length [Harrison03]. The various steps employed during the fabrication of SON DG MOSFET are: Step 1: A two step epitaxy process (after STI formation) i.e. selective epitaxy of SiGe followed by non selective epitaxy of silicon is performed for well controlled channel thickness. Step 2: Source, drain and channel region is formed followed by Reactive Ion Etching (RIE) of Si/SiGe stack layer. Step 3: Thick
A layer of gate oxide is grown over the remaining silicon layer. **Step 4:** Top and bottom gate are patterned by RIE gate etch. SON DG MOSFET fabricated from the above mentioned steps is also suffers from serious drawback i.e. the bottom gate under the source and drain region leads to higher overlap capacitance which degrades the dynamic performance of the device. Thus in ESDG MOSFET empty space layer is introduced in between the channel of DG MOSFET so that the parasitic capacitance along with the SCEs, are suppressed.

In 2007, Chung, *et al.* demonstrated the fabrication feasibility of Double Gate SOI (DGSOI) MOSFET using a new alternative approach based on the wafer bonding of a thin silicon layer over pre-etched cavity [Chung07]. The basic principle for fabricating the DGSOI MOSFET consists of 1) fabrication of single gate SOI MOSFET and then flipped over the handle wafer. The silicon substrate of SOI wafer as well as the BOX is then removed to reach the silicon channel and for depositing the gate stack of the second gate i.e. the top gate. In the same year, Kilchytska *et al.* [Kilchytska07] used the same technique for fabricating SON MOSFET in which the empty layer is created in between the silicon channel region. The principle of SON process lies in the transfer of high quality thin silicon film over an array of cavities pre-etched into an oxidized silicon bulk wafer by direct wafer bonding technique [Kilchytska07].

In 2004, Lin *et al.* proposed the fabrication feasibility of long channel DG MOSFET in which semi recessed LOCOS process is used to isolate and define the bottom gate [Lin04]. By using the selective dose and energy, the degradation associated with the oxide quality is removed. Thermal oxidation is used to form the oxide of the bottom gate. After forming the bottom gate oxide, amorphous silicon is used to form the body of the double gate. To recrystallize amorphous silicon layer, nickel-induced recrystallization is used. This process is much simpler and also more flexible to fabricate wider device with asymmetric gate oxide thickness and also used to fabricate device with channel thickness below 50 nm.

On the basis of the above mentioned fabrication schemes of SON, SON DG, and DGSOI and DG MOSFET, fabrication feasibility of ESDG MOSFET seems possible in near future by using wafer bonding scheme in two steps, i.e. 1) first to make the cavity for back gate patterning and thereafter 2) empty space in between the channel region is created [Chung07], [Kilchytska07].
6.3 Calibration with Experimental Results

In absence of the experimental results of ESDG MOSFET, various models have been first calibrated with the available experimental results of ESS MOSFET fabricated by Sato et al. [Sato01]. Figure 6.03 shows the calibrated (simulated results after calibration) and the experimental results of transfer characteristics of ESS MOSFET [Sato01] for 250 nm channel length. The close proximity between simulated and the experimental results validate our model which are further used to validate analytical results.

![Figure 6.03 Experimental [Sato01] and simulated comparison of drain current in logarithmic scale for ESS MOSFET for L=250 nm, W=10 μm, tox=2.5 nm [Kumari13a].](image)

6.4 Analytical Model Formulation

A schematic cross-sectional view of a fully depleted ESDG MOSFET is shown in figure 6.04 in which Source/Drain (S/D) regions are rectangular and uniformly doped. For calculating potential in the channel region (i.e. region 2 and 4 in vertical direction), two dimensional Poisson’s equation is divided into three regions in the horizontal direction and is expressed as:

\[
\frac{\partial \varphi_{2j}^2(x, y)}{\partial x^2} + \frac{\partial \varphi_{2j}^2(x, y)}{\partial y^2} = \frac{qN_{2j}}{2\varepsilon_{2j}}, \quad 0 \leq x \leq \sum_{j=1}^{3} L_j, \quad -\left(t_2 + \frac{L_2}{2}\right) \leq y \leq -\frac{t_2}{2} \quad (6.01)
\]

where \(j=1,2,3\) stands for three different regions in horizontal direction.

Due to symmetric channel, two dimensional potential in region 2 and 4 (in vertical direction) are same.
Superposition method is used to solve (6.01) and hence the 2D Poisson’s equation is decomposed into one dimensional (1D) Poisson’s equation and two dimensional (2D) Laplace equation which satisfy the condition of the orthogonality of Fourier series [Nguyen84] [Kasturi05].

\[ \varphi_{2j}(x, y) = \varphi_{3j}(x, y) = \varphi_{L2j}(y) + \varphi_{S2j}(x, y) \]  

(6.02)

\( \varphi_{L2j}(y) \) is the one dimensional potential in the vertical direction of the channel region whereas \( \varphi_{S2j}(x, y) \) is the two dimensional potential which incorporates the effect of drain bias on the channel potential.

Figure 6.04 Schematic cross section view of the Empty space in Double Gate (ESDG) MOSFET; \( L \) is the channel length, \( L_2 \) and \( t_1 \) is the length and the thickness of empty space in the channel region and \( L_1, L_3 \) are the length of the silicon layer at the left and right side of empty space respectively, \( t_2 \) and \( t_4 \) are the thickness of silicon layer above and below the empty space layer respectively and \( t_3 \) and \( t_5 \) are the upper and lower gate oxide thickness, \( N_S^+ \) and \( N_D^+ \) are the doping of the source and drain region respectively [Kumari13a].

### 6.4.1 One Dimensional Potential Model

The solution of one dimensional Poisson’s equation in all five regions (in vertical direction) is given through (6.03a)-(6.03e).

For \( -t_3 - t_2 - \frac{t_1}{2} \leq y \leq -t_2 - \frac{t_1}{2} \) i.e., upper gate oxide region

\[ \varphi_{L3j}(y) = \frac{qN_{Sj}}{2\varepsilon_{sj}} \left( y + \frac{t_1}{2} + t_2 + t_3 \right)^2 + C_{1j} \left( y + \frac{t_1}{2} + t_2 + t_3 \right) + C_{2j} \]  

(6.03a)
For \(-\frac{t_2}{2} \leq y \leq \frac{-t_1}{2}\) i.e., upper channel region

\[
\varphi_{L2j}(y) = \frac{qN_{L2j}}{2\varepsilon_{L2j}} \left( y + \frac{t_1}{2} + t_2 \right)^2 + B_{i_j} \left( y + \frac{t_1}{2} + t_2 \right) + B_{2j}
\]  \hspace{1cm} (6.03b)

For \(-\frac{t_1}{2} \leq y \leq \frac{t_1}{2}\) i.e., empty space region

\[
\varphi_{L1j}(y) = \frac{qN_{L1j}}{2\varepsilon_{L1j}} (y)^2 + A_{i_j} (y) + A_{2j},
\]  \hspace{1cm} (6.03c)

For \(\frac{t_1}{2} \leq y \leq \frac{t_1}{2} + t_4\) i.e., lower channel region

\[
\varphi_{L4j}(y) = \frac{qN_{L4j}}{2\varepsilon_{L4j}} \left( y - \frac{t_1}{2} + t_4 \right)^2 + b_{i_j} \left( y - \frac{t_1}{2} + t_4 \right) + b_{2j}
\]  \hspace{1cm} (6.03d)

For \(\frac{t_1}{2} + t_4 \leq y \leq \frac{t_1}{2} + t_4 + t_5\) i.e., lower gate oxide region

\[
\varphi_{L5j}(y) = \frac{qN_{L5j}}{2\varepsilon_{L5j}} \left( y - \frac{t_1}{2} - t_4 - t_5 \right)^2 + c_{i_j} \left( y - \frac{t_1}{2} - t_4 - t_5 \right) + c_{2j}
\]  \hspace{1cm} (6.03e)

The Boundary conditions at the top and the bottom of ESDG MOSFET are given as:

\[
\varphi_{L3j}(y) = V_{gs} - V_{fb} \quad \text{at} \quad y = -t_3 - t_2 - \frac{t_1}{2}
\]  \hspace{1cm} (6.03f)

\[
\varphi_{L5j}(y) = V_{gs} - V_{fb} \quad \text{at} \quad y = t_5 + t_4 + \frac{t_1}{2}
\]  \hspace{1cm} (6.03g)

The various constants in (6.03a)-(6.03e) are calculated by satisfying top and bottom potential conditions given above along with the standard boundary conditions of the continuity of potential and electric field at the boundaries of different dielectrics.

\[
\varphi_{L3j}(y) = \varphi_{L2j}(y) \quad \text{and} \quad \frac{\varepsilon_{L3j}d\varphi_{L3j}(y)}{dy} = \frac{\varepsilon_{L2j}d\varphi_{L2j}(y)}{dy} \quad \text{at} \quad y = -t_3 - \frac{t_1}{2}
\]  \hspace{1cm} (6.03h)

\[
\varphi_{L2j}(y) = \varphi_{L1j}(y) \quad \text{and} \quad \frac{\varepsilon_{L2j}d\varphi_{L2j}(y)}{dy} = \frac{\varepsilon_{L1j}d\varphi_{L1j}(y)}{dy} \quad \text{at} \quad y = -\frac{t_1}{2}
\]  \hspace{1cm} (6.03i)

\[
\varphi_{L1j}(y) = \varphi_{L4j}(y) \quad \text{and} \quad \frac{\varepsilon_{L1j}d\varphi_{L1j}(y)}{dy} = \frac{\varepsilon_{L4j}d\varphi_{L4j}(y)}{dy} \quad \text{at} \quad y = \frac{t_1}{2}
\]  \hspace{1cm} (6.03j)

\[
\varphi_{L4j}(y) = \varphi_{L5j}(y) \quad \text{and} \quad \frac{\varepsilon_{L4j}d\varphi_{L4j}(y)}{dy} = \frac{\varepsilon_{L5j}d\varphi_{L5j}(y)}{dy} \quad \text{at} \quad y = \frac{t_1}{2} + t_4
\]  \hspace{1cm} (6.03k)
The constants thus obtained using above boundary conditions (6.03f)-(6.03k) are summarized in Table 6.01.

### Table 6.01 Various one dimensional constants in the vertical direction [Kumari13a].

<table>
<thead>
<tr>
<th>( C_{ij} )</th>
<th>( \frac{\varepsilon_{2j}}{\varepsilon_{s_j}} B_{ij} - \frac{qN_{3j}t_3}{\varepsilon_{s_j}} )</th>
<th>( C_{2j} = V_{gs} - V_{fb} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( B_{ij} )</td>
<td>( \frac{\varepsilon_{1j}}{\varepsilon_{2j}} A_{ij} - \frac{qN_{3j}t_3}{\varepsilon_{2j}} )</td>
<td>( B_{2j} = \frac{qN_{3j}t_3^2}{2\varepsilon_{s_j}} + C_{1j}t_3 + C_{2j} )</td>
</tr>
<tr>
<td>( A_{ij} )</td>
<td>( P_{ij} - P_{2j} )</td>
<td>( A_{2j} = P_{2j} + A_{ij} \left( \frac{t_4}{2} + \frac{e_{1j}t_2 + e_{1j}t_3}{e_{s_j}} \right) )</td>
</tr>
<tr>
<td>( b_{ij} )</td>
<td>( \frac{\varepsilon_{1j}}{\varepsilon_{s_j}} A_{ij} + \frac{qN_{3j}t_3}{\varepsilon_{s_j}} )</td>
<td>( b_{2j} = \frac{qN_{3j}t_3^2}{2\varepsilon_{s_j}} - e_{1j}t_5 + c_{2j} )</td>
</tr>
<tr>
<td>( c_{ij} )</td>
<td>( \frac{\varepsilon_{s_j}}{e_{s_j}} b_{ij} + \frac{qN_{3j}t_3}{e_{s_j}} )</td>
<td>( c_{2j} = V_{gs} - V_{fb} )</td>
</tr>
</tbody>
</table>

The coefficients \( P_{ij} \) and \( P_{2j} \) in Table 6.01 are given as:

\[
P_{ij} = V_{gs2} - V_{fb2} - \frac{qN_{1j} \left( \frac{t_4}{2} \right)^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}l_5^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_3^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_4 \left( \frac{t_4}{2} \right)}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_5 \left( \frac{t_4}{2} \right)}{2\varepsilon_{s_j}} - \frac{qN_{3j}l_5 t_3}{2\varepsilon_{s_j}} (6.04)
\]

\[
P_{2j} = V_{gs1} - V_{fb1} - \frac{qN_{1j} \left( \frac{t_4}{2} \right)^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}l_5^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_3^2}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_4 \left( \frac{t_4}{2} \right)}{2\varepsilon_{s_j}} - \frac{qN_{3j}t_5 \left( \frac{t_4}{2} \right)}{2\varepsilon_{s_j}} - \frac{qN_{3j}l_5 t_3}{2\varepsilon_{s_j}} (6.05)
\]

### 6.4.2 Two Dimensional Potential Model

Two dimensional channel potential \( \varphi_{S2j}(x,y) \) is obtained by solving Laplace equation expressed as:

\[
\frac{\partial^2 \varphi_{S2j}(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_{S2j}(x,y)}{\partial y^2} = 0, \quad 0 \leq x \leq \sum_{j=1}^{3} L_{ij}, \quad t_2 - t_1 \leq y \leq \frac{t_1}{2} (6.06)
\]

In order to solve the boundary value problem by superposition method, the two dimensional electrostatic potential \( \varphi_{S2j}(x,y) \) given above is decomposed into the following terms:

\[
\varphi_{S2j}(x,y) = U_{li}(x,y) + U_{ri}(x,y) \quad 0 \leq x \leq \sum_{j=1}^{3} L_{ij} (6.07a)
\]
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where $U_{Lj}(x,y)$ and $U_{Rj}(x,y)$ are the solutions [Lee04] satisfying the left side and right side boundary conditions respectively in three different channel regions and are expressed as:

$$U_{Lj}(x,y) + U_{Rj}(x,y) = \left[ \sum_{n=1}^{\infty} b_{2j} \frac{\sinh \left( K_{nj} \left( \sum_{j=1}^{3} L_j - x \right) \right)}{\sinh \left( K_{nj} \sum_{j=1}^{3} L_j \right)} \right] + \left[ \sum_{n=1}^{\infty} c_{2j} \frac{\sinh \left( K_{nj} \left( \sum_{j=1}^{3} x \right) \right)}{\sinh \left( K_{nj} \sum_{j=1}^{3} L_j \right)} \right] \sin \left( K_{nj} \left( y + \frac{t_1}{2} + t_2 \right) + \beta_{2j} \right) \forall \ 0 \leq x \leq \sum_{j=1}^{3} L_j$$

(6.07b)

where $K_{nj} = n \pi \lambda_{nj}$ and $\lambda_{nj}$ is the characteristic length of the device, obtained by satisfying the continuity of the electric field and potential across the boundary of two dielectrics [Frank98]. The resulting eigenvalue equation of $K_{nj}$ in ESDG MOSFET is given as:

$$\cot \left( \frac{\pi}{\lambda_{nj}} \right) = \frac{b_{2j} \tan \left( \frac{\pi}{\lambda_{nj}} t_3 \right) \tan \left( \frac{\pi}{\lambda_{nj}} t_2 \right)}{1 - b_{2j} \tan \left( \frac{\pi}{\lambda_{nj}} t_3 \right) \tan \left( \frac{\pi}{\lambda_{nj}} t_2 \right)} = \frac{c_{2j} \tan \left( \frac{\pi}{\lambda_{nj}} t_3 \right)}{\varepsilon_{3j}} + \frac{c_{2j} \tan \left( \frac{\pi}{\lambda_{nj}} t_2 \right)}{\varepsilon_{2j}} \quad (6.08)$$

where $\beta_{2j}$ in (6.07b) is given as:

$$\beta_{2j} = a \tan \left( \frac{\varepsilon_{2j} \tan \left( K_{nj} t_3 \right)}{\varepsilon_{3j}} \right) \quad (6.09a)$$

$\beta_{2j}$ is obtained by satisfying the condition given as:

$$U_{Lj}(0,y) = U_{Rj}(L,y) = 0 \text{ at } y = \frac{t_1}{2} - t_2 - t_3 \text{ and } y = \frac{t_1}{2} + t_4 + t_5 \quad (6.09b)$$

$\beta_{3j} = 0$ at $y = \frac{t_1}{2} - t_2 - t_3 \quad (6.09c)$

$\beta_{5j} = n \pi$ at $y = \frac{t_1}{2} + t_4 + t_5 \quad (6.09d)$

The boundary conditions at the side walls of the channel i.e. at the source and drain side are given as:

$$\phi_{2j}(0,y) = V_{bi} \bigg|_{y=0} \quad (6.10a)$$

$$\phi_{2j}(L,y) = V_{bi} + V_{de} \bigg|_{x=L} \quad (6.10b)$$
The constants at the source side \((b_{21})\) and at the drain side \((c_{22})\) are obtained by using the above boundary conditions with the orthogonality of the Fourier series and comes out to be as:

\[
b_{21} = \frac{H_{1n} + H_{2n}}{t_2 + \sin(2\beta_{21}) + \sin(2(K_{n1} + \beta_{21}))} \tag{6.11}
\]

\[
c_{23} = \frac{H_{1dn} + H_{2dn}}{t_2 + \sin(2\beta_{23}) + \sin(2(K_{n3} + \beta_{23}))} \tag{6.12}
\]

Various terms \(H_{1n}, H_{2n}, H_{1dn}\) and \(H_{2dn}\) in the above equation are given as:

\[
H_{1n} = \cos(\beta_{21}) \left[ \frac{V_{bi}}{K_{n1}} + \frac{qN_{21}}{\varepsilon_1 K_{n1}^3} - \frac{B_{21}}{K_{n1}} \right] + \cos(K_{n1}t_2 + \beta_{21}) \left[ \frac{qN_{23}t_2^2}{2\varepsilon_3 K_{n1}} - \frac{V_{bi}}{K_{n1}} + \frac{qN_{21}}{\varepsilon_2 K_{n1}^3} + \frac{B_{21}t_2}{K_{n1}} + \frac{B_{1}t_3}{K_{n1}} \right] \tag{6.13a}
\]

\[
H_{2n} = \sin(\beta_{21}) \left[ \frac{B_{11}}{K_{n1}^2} \right] - \sin(K_{n1}t_2 + \beta_{21}) \left[ \frac{qN_{23}t_2^2}{2\varepsilon_3 K_{n1}} + \frac{B_{11}}{K_{n1}} \right] \tag{6.13b}
\]

\[
H_{1dn} = \cos(\beta_{23}) \left[ \frac{V_{bi} + V_{ds}}{K_{n3}} + \frac{qN_{23}}{\varepsilon_3 K_{n3}^3} - \frac{B_{23}}{K_{n3}} \right] + \cos(K_{n3}t_2 + \beta_{23}) \left[ \frac{qN_{23}t_2^2}{2\varepsilon_3 K_{n3}} - \frac{V_{bi} + V_{ds}}{K_{n3}} - \frac{qN_{23}}{\varepsilon_3 K_{n3}^3} - \frac{B_{23}t_2}{K_{n3}} + \frac{B_{1}t_3}{K_{n3}} \right] \tag{6.13c}
\]

\[
H_{2dn} = \sin(\beta_{23}) \left[ \frac{B_{13}}{K_{n3}^2} \right] - \sin(K_{n3}t_2 + \beta_{23}) \left[ \frac{qN_{23}t_2^2}{2\varepsilon_3 K_{n3}} + \frac{B_{13}}{K_{n3}} \right] \tag{6.13d}
\]

The other four constants in the center of the channel region (i.e. \(c_{21}, b_{22}, c_{22}, \) and \(b_{23}\)) are calculated by satisfying the standard boundary conditions of continuity of electric flux and potential at the different interfaces i.e., at \(L_1\) and \(L_2\) and are given as:

\[
c_{22} = \left[ \frac{P_3}{\tanh(K_{n2}L_1)} + \frac{P_1}{\tanh(K_{n1}L_1)} \right] + \left[ \frac{P_3}{\tanh(K_{n2}L_3)} + \frac{P_1}{\tanh(K_{n1}L_3)} \right] + A \left[ \frac{P_3}{\tanh(K_{n2}L_1)} + \frac{P_1}{\tanh(K_{n1}L_1)} \right] \tag{6.14a}
\]

The various terms i.e. \(A, B, E, P_1, P_2, P_3, P_4\) and \(P_5\) used in the above equation are given as:

\[
A = \cosh(K_{n2}L_2) + \frac{\sinh(K_{n2}L_2)}{\tanh(K_{n1}L_1)} \tag{6.14b}
\]
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\[
B = \begin{pmatrix}
-\cosh(K_n L_1) \tanh(K_n L_1) + \sinh(K_n L_1) \sinh(K_n L_3) \\
+ (\sinh(K_n L_3) + \cosh(K_n L_3) \tanh(K_n L_3)) \left( \cosh(K_n (L_1 + L_2)) \sinh(K_n L_3) + \sinh(K_n (L_1 + L_2)) \cosh(K_n L_3) \right)
\end{pmatrix}
\sinh(K_n (L_1 + L_2)) \sinh(K_n L_3) \tanh(K_n L_3)
\]

\[E = \frac{1}{2} \left[ t_2 - \frac{\sin(2\beta_{22})}{2K_n} - \frac{\sin(2(K_n t_2 + \beta_{22}))}{2K_n} \right] \]  

(6.14c)

\[P_1 = Q_{1n} + Q_{2n} - Q_{3n} - Q_{4n} \]  

(6.14d)

\[P_2 = Q_{3n} + Q_{4n} - Q_{in} - Q_{2n} \]  

(6.14e)

\[P_3 = \frac{b_{21} P}{\sin(K_n L_1)} \]  

(6.14f)

\[P_4 = \frac{c_{23} P \sinh(K_n (L_1 + L_2))}{\sin(K_n L_1)} \]  

(6.14g)

\[P_5 = \frac{c_{23} P \cosh(K_n (L_1 + L_2))}{\sin(K_n L_1)} \]  

(6.14h)

\[Q_{1n}, Q_{2n}, Q_{3n} \text{ and } Q_{4n} \text{ in (6.14e) and (6.14f) are given as:} \]

\[Q_{4n} = \cos(\beta_{22}) \left[ \frac{-qN_{22}}{\varepsilon_{22} K_n^3} + \frac{B_{22}}{K_n^2} \right] + \cos(K_n t_2 + \beta_{22}) \left[ \frac{-qN_{22} t_2^2}{2\varepsilon_{22} K_n^2} + \frac{qN_{22}}{\varepsilon_{22} K_n^3} - \frac{B_{22}}{K_n} - \frac{B_{23} t_2}{K_n^2} \right] \]  

(6.14i)

\[Q_{2n} = -\sin(\beta_{22}) \left[ \frac{B_{11}}{K_n^2} \right] + \sin(K_n t_2 + \beta_{22}) \left[ \frac{qN_{22} t_2^2}{2\varepsilon_{22} K_n^2} + \frac{B_{11}}{K_n^2} \right] \]  

(6.14j)

\[Q_{3n} = \cos(\beta_{22}) \left[ \frac{-qN_{22}}{\varepsilon_{22} K_n^3} + \frac{B_{22}}{K_n^2} \right] - \cos(K_n t_2 + \beta_{22}) \left[ \frac{qN_{22} t_2^2}{2\varepsilon_{22} K_n} - \frac{qN_{22}}{\varepsilon_{22} K_n^3} + \frac{B_{22}}{K_n^2} + \frac{B_{23} t_2}{K_n^2} \right] \]  

(6.14k)

\[Q_{4n} = \sin(\beta_{22}) \left[ \frac{-B_{11}}{K_n^2} \right] + \sin(K_n t_2 + \beta_{22}) \left[ \frac{qN_{22} t_2^2}{2\varepsilon_{22} K_n} + \frac{B_{11}}{K_n^2} \right] \]  

(6.14l)

\[b_{22} = \frac{\sinh(K_n (L_1 + L_2))}{E} \left[ \frac{c_{22} E}{\left( \tan (K_n (L_1 + L_2)) + \frac{1}{\tan (K_n L_3)} \right)} - \left( \frac{P_2}{\tan (K_n L_3)} + \frac{P_3}{\tan (K_n L_3)} + \frac{P_4}{\tan (K_n L_3)} \right) \right] \]  

(6.15)

\[P_1 = Q_{1n} + Q_{2n} - Q_{3n} - Q_{4n} \]  

(6.14m)

\[P_2 = Q_{3n} + Q_{4n} - Q_{in} - Q_{2n} \]  

(6.14n)
\[ b_{23} = \frac{c_{22} P - P_{a1} - P_{21} \sinh(K_{n1} L_2)}{\tanh(K_{n1} L_3) E_i} \]  

(6.16a)

The various terms i.e. \( P, P_{a1}, P_{21}, \) and \( E_i \) used in the above equation (6.16a) are given as:

\[ P = \frac{1}{2} \left[ \frac{\sin((-K_{n2} - K_{n1}) t_1 + (-\beta_{21} + \beta_{22}))}{-K_{n1} + K_{n2}} - \frac{\sin((K_{n2} + K_{n1}) t_1 + (\beta_{21} + \beta_{22}))}{K_{n1} + K_{n2}} \right] \]  

(6.16b)

\[ P_{a1} = \frac{b_{23} \sinh(K_{n1} (L_1 + L_2))}{2 \sinh(K_{n1} (L))} \left[ t_2 - \frac{\sin(2 \beta_{23})}{2 K_{n1}} - \frac{\sin(2 (K_{n1} t_2 + \beta_{21}))}{2 K_{n1}} \right] \]  

(6.16c)

\[ E_i = \frac{1}{2} \left[ t_2 - \frac{\sin(2 \beta_{23})}{2 K_{n1}} - \frac{\sin(2 (K_{n1} t_2 + \beta_{21}))}{2 K_{n1}} \right] \]  

(6.16d)

\[ P_{21} = R_{3n} + R_{4n} - R_{in} - R_{2n} \]  

(6.16e)

\( R_{in}, R_{2n}, R_{3n}, \) and \( R_{4n} \) in the above are given as:

\[ R_{in} = \cos(\beta_{21}) \left[ -\frac{q N_{21}}{\varepsilon_1 K_{n1}^3} + \frac{B_{22}}{K_{n1}} \right] + \cos(K_{n1} t_2 + \beta_{21}) \left[ -\frac{q N_{21} t_2^2}{2 \varepsilon_2 K_{n1}^3} + \frac{q N_{21}}{2 \varepsilon_2 K_{n1}^3} + \frac{B_{22}}{K_{n1}} - \frac{B_{23} t_2}{K_{n1}} \right] \]  

(6.16f)

\[ R_{2n} = -\sin(\beta_{21}) \left[ \frac{B_{21}}{K_{n1}^2} + \sin(K_{n1} t_2 + \beta_{21}) \left[ \frac{q N_{21} t_2^2}{\varepsilon_2 K_{n1}^2} + \frac{B_{22}}{K_{n1}} \right] \right] \]  

(6.16g)

\[ R_{3n} = \cos(\beta_{21}) \left[ -\frac{q N_{21}}{\varepsilon_1 K_{n1}^3} + \frac{B_{22}}{K_{n1}} \right] - \cos(K_{n1} t_2 + \beta_{21}) \left[ \frac{q N_{21} t_2^2}{2 \varepsilon_2 K_{n1}^3} + \frac{q N_{21}}{2 \varepsilon_2 K_{n1}^3} + \frac{B_{22}}{K_{n1}} - \frac{B_{23} t_2}{K_{n1}} \right] \]  

(6.16h)

\[ R_{4n} = \sin(\beta_{21}) \left[ -\frac{B_{21}}{K_{n1}^2} + \sin(K_{n1} t_2 + \beta_{21}) \left[ \frac{q N_{21} t_2^2}{\varepsilon_2 K_{n1}^2} + \frac{B_{22}}{K_{n1}} \right] \right] \]  

(6.16i)

\[ c_{21} = \frac{b_{22} P \sinh(K_{n2} L_2) + \sinh(K_{n2} L_1)}{\sinh(K_{n2} (L_1 + L_2)) + \sinh(K_{n2} (L_1 + L_2)) + P_{a1}} E_i \]  

(6.17a)
where \( P_{11} \) in the (6.17a) is given as:

\[
P_{11} = R_{1n} + R_{2n} - R_{3n} - R_{4n}
\]

(6.17b)

In the next section, drain current for ESDG MOSFET has been examined by dividing it into three regions i.e. 1) Sub-threshold region for \( V_{gs} < V_{th} \) and \( V_{ds} < V_{dsat} \) 2) Linear Region for \( V_{gs} > V_{th} \) and \( V_{ds} < V_{dsat} \) and 3) saturation region for \( V_{gs} > V_{th} \) and \( V_{ds} > V_{dsat} \).

6.4.3 Sub-threshold Region Drain Current Model

Only diffusion current component is considered in the channel region to model the sub-threshold drain current. Using two dimensional potential in the channel region, sub-threshold current is calculated analytically by integrating channel potential over the entire channel region twice without using any fitting parameter [Hariharan09] as a function of \( V_{gs} \) and \( V_{ds} \).

In the present analysis, empty space layer is present in between the channel region and hence two separate channel regions are formed. The total current in the device is the sum of current in two individual channels. Sub-threshold current in the upper channel region \((t_2)\) is given as:

\[
I_{ds2} = \mu W \left( \frac{kT}{q} \right) \left[ 1 - \exp \left( \frac{-qV_{ds}}{kT} \right) \right]
\]

\[
\int_{t_2}^{t_1} \frac{1}{I_{21}(x,y)} \, dx + \int_{t_1}^{t_1+t_2} \frac{1}{I_{22}(x,y)} \, dx + \int_{t_1+t_2}^{t_1+t_2+t_2} \frac{1}{I_{23}(x,y)} \, dx
\]

(6.18a)

where \( I_{21}(x,y) \), \( I_{22}(x,y) \) and \( I_{23}(x,y) \) in the above equation are given as:

\[
I_{21}(x,y) = \int_{-\frac{L}{2}}^{\frac{L}{2}} n_q \exp \left( \varphi_{21} (x,y) \right) \, dy
\]

(6.18b)

\[
I_{22}(x,y) = \int_{-\frac{L}{2}}^{\frac{L}{2}} n_q \exp \left( \varphi_{22} (x,y) \right) \, dy
\]

(6.18c)

\[
I_{23}(x,y) = \int_{-\frac{L}{2}}^{\frac{L}{2}} n_q \exp \left( \varphi_{23} (x,y) \right) \, dy
\]

(6.18d)
Sub-threshold current in the lower channel region \((t_4)\) is given as:

\[
I_{d4} = \mu W \left( \frac{kT}{q} \right) \left[ 1 - \exp \left( -\frac{qV_{ds}}{kT} \right) \right] \int_0^{t_4} \left[ \frac{1}{I_{d1}(x,y)} \right] dx + \int_{t_4}^{t_4+t_L} \left[ \frac{1}{I_{d2}(x,y)} \right] dx + \int_{t_4+t_L}^{t_4+L} \left[ \frac{1}{I_{d3}(x,y)} \right] dx
\]

where \(I_{d1}(x,y), I_{d2}(x,y)\) and \(I_{d3}(x,y)\) in the above equation are given as:

\[
I_{d1}(x,y) = \int_{\frac{L}{2}}^{\frac{L}{2}+t_4} n_i q \exp\left( \varphi_{d1}(x,y) \right) dy
\]

\[
I_{d2}(x,y) = \int_{\frac{L}{2}}^{\frac{L}{2}+t_4+t_L} n_i q \exp\left( \varphi_{d2}(x,y) \right) dy
\]

\[
I_{d3}(x,y) = \int_{\frac{L}{2}}^{\frac{L}{2}+t_4+t_L} n_i q \exp\left( \varphi_{d3}(x,y) \right) dy
\]

Hence the total sub-threshold drain current is \(I_{ds} = I_{ds2} + I_{ds4}\) \((6.20)\)

While calculating the sub-threshold current, it is assumed that the gate leakage current is negligible in ESDG MOSFET. \(W\) is the channel width, \(L\) is the total channel length, \(k\) is the Boltzmann’s constant, \(T\) is the operating temperature, \(n_i\) is the intrinsic carrier concentration. \(\mu\) is the temperature dependent charge carriers mobility calculated from the Arora model discussed in chapter 2.

For an ideal switch, sub-threshold current should go abruptly to zero for \(V_{gs} < V_{th}\).

However in ideal, case sub-threshold slope \((S)\) is the determining factor in characterizing the on-off switching behavior of CMOS \([Bhattacharyya09]\) which is defined as:

\[
S = \ln(10) \frac{\partial V_{gs}}{\partial \ln(I_{ds})} = I_{ds} \ln(10) \left[ \frac{\partial(I_{ds})}{\partial V_{gs}} \right]^{-1}
\]

where \(I_{ds}\) is the total sub-threshold drain current given above.
6.4.4 Drain Current Model in Linear Region

The drain current in the linear region is calculated by using charge control model under gradual channel approximation and is expressed as [Kaur09]:

\[
I_{ds,lin} = \frac{\mu W (C_{ox}) \left( (V_{gs} - V_{th}) V_{ds} - 0.5 a_o V_{ds}^2 \right)}{1 + \frac{V_{ds}}{L E_c}} L \tag{6.22a}
\]

\(C_{ox}\) and \(E_c\) are the gate oxide capacitance and temperature dependent critical electric field respectively and are given as:

\[
C_{ox} = \frac{\varepsilon_s}{t_3} \tag{6.22b}
\]

\[
E_c = \frac{V_{sat}}{\mu} \tag{6.22c}
\]

\(V_{sat}\) is the saturation velocity taken as \(1.03 \times 10^7 \) cm s\(^{-1}\). \(a_o\) in (6.22a) is the coefficient accounting for DIBL effect [Lim84] and is given as:

\[
a_o = 1 + \frac{\varepsilon_s}{t_2 C_{ox}} \tag{6.22d}
\]

6.4.5 Drain Current Model in Saturation Region

Drain current equation in saturation region \(I_{ds, sat}\) incorporating various SCEs like Channel Length Modulation (CLM) and velocity overshoot effect is modeled in this section. The saturation drain current is given as [Lim02] [Kaur07a]:

\[
I_{ds, sat} = \frac{\mu W (C_{ox}) \left( (V_{gs} - V_{th}) V_{ds, sat} - 0.5 a_o V_{ds, sat}^2 \right)}{1 + \frac{V_{ds, sat}}{(L - L_e) E_c + h E_c (L - L_e) (V_{ds} - V_{ds, sat}) (L - L_e)}} \tag{6.23a}
\]

Velocity overshoot (higher drift velocity than saturation velocity) is a non-local effect mainly arises because of high electric field at the drain side which enhances the drain current with increasing drain bias conventionally modeled by CLM effect [Lim02] [Kaur07a]. \(L_e\) is the length of velocity saturation region due to Channel Length Modulation (CLM) given as:

\[
L_e = l \ln \left[ \frac{V_{ds} - V_{ds, sat}}{l E_c} + \frac{E_m}{E_c} \right] \tag{6.23b}
\]
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$E_m$ is the maximum electric field given by:

$$E_m = E_c \sqrt{1 + \left[\frac{V_{ds} - V_{d_{sat}}}{IE_c}\right]^2}$$  \hspace{1cm} (6.23c)

$$l = \sqrt{\frac{E_2}{E_3}} (t_2 t_3)$$  \hspace{1cm} (6.23d)

$V_{d_{sat}}$ is the drain saturation voltage given as:

$$V_{d_{sat}} = \frac{V_{gs} - V_{th}}{1 + \frac{V_{gs} - V_{th}}{IE_c}}$$  \hspace{1cm} (6.23e)

$h$ in (6.23a) is used to model the saturation field and is given as:

$$h = \frac{\zeta \left(\frac{c}{l^2}\right)}{\sqrt{1 + \left[\frac{V_{ds} - V_{d_{sat}}}{IE_c}\right]^2}} \left[1 + \sqrt{1 + \left[\frac{V_{ds} - V_{d_{sat}}}{IE_c}\right]^2}\right] \hspace{1cm} (6.23f)$$

$$c = \frac{2kT_L \mu}{d}$$  \hspace{1cm} (6.23g)

Where $\zeta$ in (6.23f) is an added constant (fitting parameter) used to adjust the $l$ to match the peak channel field and $T_L$ is the lattice temperature [Kaur07a].

6.5 Model Validation with Simulation Results

The various parameters used for simulating the ESDG MOSFET are taken as: channel doping ($N_2=N_4$) is $10^{21}$ m$^{-3}$, $N_1$, $N_3$ and $N_5$ are the doping of empty space layer, upper and lower gate oxide regions respectively and are taken as zero. The S/D regions are heavily doped with doping $N_D = N_3 = 10^{26}$ m$^{-3}$. The channel length of the ESDG MOSFET has been varied from 120 nm to 30 nm at two different channel thicknesses i.e. $t_{si}=30$ nm and $t_{si}=20$ nm. In both cases, thickness of empty space layer is kept constant i.e. 10 nm. The silicon film thickness ($t_2=t_4$) on both the side of empty space layer is 5 nm when $t_{si}=10$ nm and 10 nm when $t_{si}=30$ nm. The thickness of the upper and lower gate oxide thickness is also varied from 3 nm to 2 nm.
Various models invoked during device simulation are transverse field dependent (FLDMOB) mobility and Arora mobility model. Shockley-Read-Hall (SRH) and Auger recombination models are also used \textit{[ATLAS10]}. The physics behind various models invoked during simulation of non-classical devices are already discussed in detail \textit{in chapter 3}. Since Quantum effects are significant for channel thicknesses smaller than 5 nm and for channel lengths below 10 nm \textit{[Querlioz07]} and thus obscuring its inclusion in the present analysis. Moreover, the good agreement between drain current with and without using quantum model \textit{in chapter 5} at 60 nm channel length also validates our assumption of non-inclusion of quantum effects.

\subsection*{6.5.1 Drain Current}

\textit{In this sub-section}, drain current i.e. transfer characteristics and output characteristics of various devices have been compared through exhaustive device simulation. The impact of parametric variations i.e. channel thickness ($t_{si}$) and channel length ($L$) on the drain current of ESDG MOSFET have also been investigated using analytical modeling.

Figure 6.05 (a) illustrates that with increasing channel thickness, off-state leakage current ($I_{off}$) of the device also increases i.e. 76% in ESDG MOSFET.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure6.05}
\caption{Transfer characteristics in logarithmic scale for different (a) channel thickness ($t_{si}$) and (b) channel length ($L$); for L=90 nm ($L_1=30$ nm and $L_2=30$ nm), for L=60 nm ($L_1=20$ nm and $L_2=20$ nm), remaining parameters are: $V_{ds}=0.1$ V, $t_1=10$ nm, $t_2=t_3=2$ nm, $q\Phi_m=4.77$ eV and $T=300$ K \textit{[Kumari13a]}.}
\end{figure}
It can also be observed from figure 6.05 (a) that, ESDG MOSFET exhibits lower leakage current ($I_{off}$) at 90 nm channel length as compared to ESS (66%) and DG (58%) MOSFET. 

Figure 6.05 (b) shows that, suppression in off state current ($I_{off}$) in ESDG MOSFET as compared to Bulk ESS and DG MOSFET at 60 nm channel length is 97% and 93% respectively. This is only because of the reduced electrostatic coupling between the source drain regions due to the presence of empty space layer in the channel. This implies that, ESDG MOSFET exhibits higher immunity against the channel length scaling as compared to DG and ESS MOSFET. The results also show that ESDG MOSFET exhibits lower sub-threshold slope as compared to ESS (30%) and DG (3%) MOSFET and thereby showing suppression in SCEs. The enhancement in sub-threshold slope with channel length scaling is also lower in ESDG MOSFET i.e. 3.2% however it is 8% in DG and 34% in ESS MOSFETs.

Figure 6.06 illustrates the impact of channel length on $I_{ds}$-$V_{ds}$ of ESDG MOSFET and the good agreement between simulated and the analytical results are observed. As the channel length decreases, drain current $I_{ds}$ increases (39%) and also the change in drain current with applied drain bias is negligible in ESDG MOSFET thereby showing lower Channel Length Modulation (CLM) effect. This is because of the reduction in the electrostatic coupling between highly doped source drain regions in ESDG MOSFET even at the lower channel length.

**Figure 6.06** Output characteristics of ESDG MOSFET at different channel lengths i.e. $L=90$ nm ($L_1=30$ nm and $L_2=30$ nm), for $L=60$ nm ($L_1=20$ nm and $L_2=20$ nm); $V_{gs}=1.0$ V, $t_1=10$ nm, $t_2=t_4=5$ nm, $t_3=t_5=2$ nm, and $q\Phi_m=4.77$ eV [Kumari13a].
6.5.2 Threshold Voltage

In this section, the impact of device parameters (like channel thickness \( t_{si} \) and gate oxide thickness \( t_{3}=t_{5} \)) on the threshold voltage roll-off of different devices have been investigated. The threshold voltages of the different devices are calculated from the Constant Current (CC) method as discussed in chapter 2.

![Graph showing threshold voltage and DIBL variation with channel length for different device configurations.](image)

**Figure 6.07** Variation of Threshold voltage and DIBL with channel length (a) for different channel thickness \( t_{si}=t_{3}=2 \text{ nm, } q\Phi_{m}=4.77 \text{ eV} \) (b) for different gate oxide thickness for \( t_{1}=10 \text{ nm, } t_{2}=t_{4}=5 \text{ nm, } q\Phi_{m}=4.77 \text{ eV} \) and \( V_{ds}=0.5 \text{ V} \) [Kumari13a].
As channel length decreases, potential barrier at the source side of the MOSFET also decreases. This is due to the enhancement in lateral field penetration from drain to source and thereby showing reduction in the threshold voltage as shown in figure 6.07 (a) and (b). Results also show that, ESDG MOSFET has lower threshold voltage roll off as compared to bulk ESS and DG MOSFETs because of the presence of Empty Space layer that can eliminate the coupling path between S/D regions [Tian05]. As the channel thickness decreases in figure 6.07 (a), electrostatic coupling between two gates increases and hence the influence drain bias at the source side reduces, thereby showing effective improvement in the scaling capability of ESDG MOSFET. As the channel thickness decreases, DIBL effect of the device also decreases. The enhancement in DIBL effect can also be observed from the figure with the channel length scaling.

Figure 6.07 (b) shows that, as the gate oxide thickness increases, the effective gate control over the channel region decreases, resulting in the enhancement in threshold voltage. Also the threshold voltage roll-off with channel length is lower in ESDG as compared to ESS and DG i.e. ~60% from ESS and ~38% from DG MOSFET. It is also evident from the figure that threshold voltage roll-off with channel length is more prominent in the device having thicker gate oxide region.

![Figure 6.08 Threshold voltage roll off with channel length for different metal gate work-function; $t_1=10$ nm, $t_2=k_4=5$ nm and $V_{dd}=0.5$ V [Kumari13a].](image)

**Figure 6.08** Threshold voltage roll off with channel length for different metal gate work-function; $t_1=10$ nm, $t_2=k_4=5$ nm and $V_{dd}=0.5$ V [Kumari13a].
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The impact of metal-gate work function on the threshold voltage of ESDG MOSFET is demonstrated in figure 6.08. As the metal gate work-function ($\Phi_m$) increases, effective gate voltage which appears on the surface of channel decreases (i.e. $V_{gs}-V_{fb}$) leading to threshold voltage enhancement. This is so because, as metal gate work function ($\Phi_m$) increases, barrier height ($\Phi_m-\Phi_s$) at the SiO$_2$/Si interface increases thereby showing enhancement in $V_{th}$. Figure 6.08 also shows lower threshold voltage roll-off, with increase in metal gate work-function.

6.5.3 Impact of Empty Space Layer on Electrical Parameters

In this section, impact of the length of empty space layer ($L_2$) on electrical performance of ESDG MOSFET has been analyzed. Table 6.02 illustrates that, as the length of empty space layer ($L_2$) increases, 75% reduction in DIBL is observed. In addition, there is marginal change in sub-threshold slope (2%) of ESDG MOSFET with the change in length of empty space layer ($L_2$). However, the reduction in sub-threshold slope in ESDG MOSFET as compared to DG is higher at shorter gate length as already discussed previously. As $L_2$ increases, threshold voltage ($V_{th}$) of the device also increases due to reduced electrostatic coupling between the drain and the source region. The 13% reduction in leakage current ($I_{off}$) can also be observed with the enhancement in $L_2$. Thus, from the data given in the Table 6.02 it was found that the optimum value of empty space layer in ESDG MOSFET for better device performance is 70 nm for 90 nm channel length.

Table 6.02 Analytical and simulated electrical parameters of ESDG MOSFET at different length of empty space layer ($L_2$) [Kumari13a].

<table>
<thead>
<tr>
<th>at $V_{ds}=0.5$ V</th>
<th>$L_2=70$ nm</th>
<th>$L_2=50$ nm</th>
<th>$L_2=30$ nm</th>
<th>$L_2=10$ nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th}$ (V)</td>
<td>Sim. 0.404</td>
<td>0.401</td>
<td>0.385</td>
<td>0.37</td>
</tr>
<tr>
<td></td>
<td>Ana. 0.406</td>
<td>0.402</td>
<td>0.392</td>
<td>0.39</td>
</tr>
<tr>
<td>$S$ (mV/decade)</td>
<td>Sim. 60.01</td>
<td>60.11</td>
<td>60.31</td>
<td>61.49</td>
</tr>
<tr>
<td></td>
<td>Ana. 60.37</td>
<td>60.42</td>
<td>60.61</td>
<td>60.71</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>Sim. 5.00</td>
<td>7.50</td>
<td>12.50</td>
<td>20.00</td>
</tr>
<tr>
<td></td>
<td>Ana. 6.25</td>
<td>8.00</td>
<td>12.50</td>
<td>17.50</td>
</tr>
<tr>
<td>$I_{off}$ (pA)</td>
<td>Sim. 0.176</td>
<td>0.202</td>
<td>0.269</td>
<td>0.466</td>
</tr>
<tr>
<td></td>
<td>Ana. 0.224</td>
<td>0.269</td>
<td>0.273</td>
<td>0.598</td>
</tr>
</tbody>
</table>

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6.6 Impact of Temperature Variation

As discussed in chapter 2 and 5, there are various applications that demand for integrated circuits operating at high temperature. However, at nanoscale region the SCEs are the major bottleneck associated with the performance of MOSFET. Thus to achieve the stringent performance at high operating temperature with reduced SCEs, different non-classical devices such as SOI and SON MOSFET have been discussed in the literature. As discussed previously, the variation in the electrical parameters are negligible with increases in operating temperature if the device is biased at the Zero Temperature Coefficient point (i.e. ZTC point) [Osman95]. In general, MOSFET has positive temperature coefficient of drain current if it is biased below ZTC and negative temperature coefficient otherwise.

In this section, impact of temperature variation on the performance of ESDG MOSFET (i.e. drain current, trans-conductance, device efficiency ($g_m/I_{ds}$), output resistance ($R_{out}$) and early voltage ($V_{ea}$)) have been investigated through exhaustive device simulation and the results are also compared with the other conventional devices. Logic circuits like NAND and NOR gate along with 3-stage ring oscillator are also realized using ESDG, ESS and DG MOSFET for propagation delay estimation and comparison which are the basic building blocks to judge the performance of the device for digital applications using ATLAS 3D mixed mode device simulator [ATLAS10].

In order to validate the simulated results for analog and digital performance at shorter gate length, calibrated models of DG MOSFET [Tsormpatzoglou09] at 60 nm channel length as discussed previously has also been used in this chapter for calibrating ESDG MOSFET. Further, Energy Balance Transport (EBT) model has been incorporated for assessing analog and digital performance of the device at higher operating temperature. The conventional drift-diffusion model of charge transport neglects the “non-local” effects such as velocity overshoot and impact ionization which are easily incorporated through the use of an EBT (which uses a higher order approximation of the Boltzmann transport equation) [ATLAS10].

In addition to this, CVT mobility model has also been invoked in the simulation. CVT model is assigned as separate model which include all the effects required for simulating the carrier mobility (i.e. temperature and field dependence of the mobility
model). The calibration of the device has also been performed in this chapter by validating the output characteristics \(I_{ds}-V_{ds}\) of the device. The close concordance among the simulation and experimental results for \(I_{ds}-V_{ds}\) in figure 6.09 validates our simulation for ESDG MOSFET.

![Figure 6.09](image)

**Figure 6.09** Experimental [Tsormpatzoglou09] and simulated output characteristics \(I_{ds}-V_{ds}\) of silicon FinFET corresponding to DG MOSFET; \(L=60\) nm, \(t_{si}\) (channel thickness)= 25 nm, \(W\) (device width)=325 nm[Kumari13a].

### 6.6.1 DC Performance

In this sub-section, impact of operating temperature on dc performance of ESDG MOSFET is analyzed by investigating drain current \(I_{ds}-V_{gs}\) and trans-conductance \(g_m\) and is also compared to DG, ESS and Bulk MOSFET as shown in figure 6.10 (a) and (b) respectively. Results show that, as the operating temperature increases, on-state current \(I_{on}\) decreases due to reduction in channel mobility at higher gate voltages. This is because of enhanced lattice scattering at higher operating temperature leading to reduction in carrier mobility. However, the leakage current is tremendously suppressed in ESDG MOSFET as compared to DG, ESS and bulk MOSFET for wide range of temperature. This is due to reduction in electrostatic coupling between drain and source regions because of the presence of empty space in silicon channel. In addition, higher drain current is achieved with ESDG MOSFET followed by DG, ESS and bulk MOSFETs. The change in \(I_{on}\) with temperature is also lower in ESDG (3%) MOSFET in comparison to DG (6%), ESS (10%) and bulk (52%) MOSFETs.
Figure 6.10 Variation of (a) drain current ($I_{ds}$) and (b) Trans-conductance ($g_m$) with gate to source voltage at different temperature; $L=60$ nm, $V_{ds}=0.5$ V, channel thickness ($t_w$) is 25 nm, gate oxide thickness ($t_{ox}$) =1.7 nm, $W=325$ nm and empty space layer thickness ($t_{box}$) is 10 nm [Kumari13b].

Figure 6.10 (b) illustrates that, ESDG MOSFET possess higher trans-conductance ($g_m$) followed by DG, ESS and bulk MOSFET. This is mainly attributed to higher drain current of ESDG MOSFET because of enhanced gate controllability and significantly suppressed coupling between the source and drain regions. At higher gate voltages, $g_m$ decreases with increase in operating temperature, however at lower gate drive voltages, $g_m$ increases with temperature. The degradation in trans-conductance with operating temperature is also lower in ESDG MOSFET as compared to DG, ESS and bulk MOSFET. This is so because the leakage current is tremendously suppressed ($I_{off}$) in ESDG MOSFET even at the higher operating temperature thereby showing better immunity against temperature variation. In order to get higher trans-conductance ($g_m$) at higher temperature, we need to bias the device below ZTC point.

6.6.2 Analog Performance

In this section, different devices are compared for the low-voltage low-power analog applications. The various parameters used to assess the performance of the device for analog applications are trans-conductance generation efficiency ($g_m/I_{ds}$), output resistance ($R_{out}$) and early voltage ($V_{ea}$).
Device efficiency \( \frac{g_m}{I_{ds}} \) also known as trans-conductance generation efficiency is an important parameter for efficient analog performance. The variation of \( g_m/I_{ds} \) with drain current of the different devices is plotted in figure 6.11. Results clearly reveal that, \( g_m/I_{ds} \) is higher for ESDG MOSFET followed by DG, ESS and bulk MOSFET. As discussed in chapter 3, the maximum value of \( g_m/I_{ds} \) in case of MOSFET is limited by 40 V\(^{-1} \). [Kilchytska07]. The detail expression of the \( g_m/I_{ds} \) for calculating its maximum value was discussed in chapter 3.

![Figure 6.11](image)

**Figure 6.11** Variation of trans-conductance generation efficiency \( (g_m/I_{ds}) \) with drain current at different operating temperature; \( V_{ds}=0.5 \) V, \( L=60 \text{ nm} \), \( t_{si}=25 \text{ nm} \), \( t_{ox}=1.7 \text{ nm} \), \( W=325 \text{ nm} \) and \( t_{box}=10 \text{ nm} \) [Kumari13b].

The observed trans-conductance generation efficiency \( g_m/I_{ds} \) of ESDG MOSFET is slightly lower than the maximum value because of nearly ideal sub-threshold slope of the device. It is also observed that, \( g_m/I_{ds} \) is maximum in sub-threshold region and decreases significantly as the drain current increases. Instead of higher drain current as well as trans-conductance of the device at higher operating temperature, the overall \( g_m/I_{ds} \) decreases with increase in operating temperature even when the device is biased below ZTC point. Also, the reduction in \( g_m/I_{ds} \) with operating temperature is lesser in ESDG MOSFET as compared to DG, ESS and bulk MOSFETs.

Another important performance metrics used to benchmark the performance for analog applications are early voltage and output resistance related to the output...
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characteristics of the device i.e. on-state current \( I_{ds} \) and drain conductance \( g_d \). For high performance analog applications, \( R_{out} \) and \( V_{ea} \) should be as high as possible \([Kaur07b]\). Figure 6.12 (a) and (b) shows the variation of output resistance \( R_{out} \) and early voltage \( V_{ea} \) respectively of different devices with applied drain bias. For high performance analog operation, lower drain-conductance \( g_d \) along with the higher drain current \( I_{ds} \) is required \([Kaur08]\). It is also evident from the results that, ESDG MOSFET exhibits higher \( R_{out} \) (i.e. 44% from DG, 64% from ESS and 81% from bulk MOSFET) and early voltage (i.e. 48% from DG, 87% from ESS and 97% from bulk MOSFET) due to the improved SCEs such as lower DIBL and CLM and is mainly attributed to lower drain-conductance \( g_d \) of the device.

![Figure 6.12](image)

**Figure 6.12** Variation of (a) Output resistance \( R_{out} \), with drain to source voltage at \( V_{gs}=0.6 \) V and (b) Early voltage with drain to source voltage \( V_{ds} \) at \( V_{gs}=1.2 \) V at different temperature; \( L=60 \) nm, \( t_{si}=25 \) nm, \( t_{ox}=1.7 \) nm, \( W=325 \) nm and \( t_{box}=10 \) nm \([Kumari13b]\).

As the temperature increases, device performance degrades due to the enhanced SCEs thereby showing reduction in output resistance and early voltage. Results also show that, ESDG MOSFET exhibits higher immunity against temperature variation as compared to DG, ESS and bulk MOSFET i.e. reduction in \( R_{out} \) and \( V_{ea} \) with operating temperature is lesser in ESDG MOSFET followed by DG, ESS and Bulk MOSFETs. This is due to enhanced gate controllability in DG and ESDG MOSFET and lower electrostatic coupling between drain and source in ESDG MOSFET as compared to ESS and bulk MOSFETs.
Table 6.03 illustrates the impact of operating temperature on the electrical performance of different devices. It can be observed that, almost ideal sub-threshold slope \((S)\) can be achieved in case of ESDG MOSFET as compared to other devices. The percentage change in sub-threshold slope with temperature is also lower in ESDG and DG followed by ESS and bulk MOSFET. ESDG MOSFET also exhibits higher device gain \((g_m/g_d)\) as compared to DG (32\%), ESS (92\%) and bulk (95\%) MOSFETs. Further, as the temperature increases, device gain decreases which is 17.9\% in ESDG, 33.3\% in DG and 33.9\% in ESS MOSFET however, it increases in case of bulk MOSFET. This is due to the fact that the device performance degrades with operating temperature at the gate bias above ZTC. The ZTC voltage of the bulk MOSFET is higher than 0.8 V thereby showing enhancement in \(g_m/g_d\) ratio with increase in operating temperature.

Table 6.03 Simulated parameters for ESDG, DG, Bulk ESS and Bulk MOSFET architectures; \(V_{dss}=0.5\) V, \(L=60\) nm, \(t_{si}=25\) nm, \(t_{ox}=1.7\) nm, \(W=325\) nm and \(t_{box}=10\) nm \([\text{Kumari13b}]\).

<table>
<thead>
<tr>
<th>Temperature in K</th>
<th>(S) (mV/dec)</th>
<th>(g_m/g_d)</th>
<th>(R_{on}) (K(\Omega))</th>
<th>(I_{on}/I_{off}) ((\times10^6))</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESDG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>63.0</td>
<td>67</td>
<td>2.01</td>
<td>47.44</td>
</tr>
<tr>
<td>400</td>
<td>85.3</td>
<td>55</td>
<td>2.2</td>
<td>0.28</td>
</tr>
<tr>
<td>DG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>71</td>
<td>45</td>
<td>2.2</td>
<td>8.86</td>
</tr>
<tr>
<td>400</td>
<td>97.13</td>
<td>30</td>
<td>2.3</td>
<td>0.10</td>
</tr>
<tr>
<td>ESS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>127.92</td>
<td>4.7</td>
<td>5.5</td>
<td>0.136</td>
</tr>
<tr>
<td>400</td>
<td>179</td>
<td>3</td>
<td>6.2</td>
<td>0.004</td>
</tr>
<tr>
<td>Bulk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>306.51</td>
<td>3.1</td>
<td>23.71</td>
<td>0.003</td>
</tr>
<tr>
<td>400</td>
<td>443.8</td>
<td>5</td>
<td>16.26</td>
<td>1.12\times10^{-4}</td>
</tr>
</tbody>
</table>

Lower \(R_{on}\) \((R_{on} \propto \frac{1}{I_{on}})\) in case of ESDG MOSFET (as shown in Table 6.03) as compared to DG (9\%), ESS (62\%) and Bulk (91\%) MOSFET is only because of the significantly high drive current. Table 6.03 also evaluates the performance of different devices in terms of \(I_{on}/I_{off}\) ratio and it can be observed that higher \(I_{on}/I_{off}\) ratio can be achieved with ESDG MOSFET followed by DG, ESS and bulk MOSFET. The degradation in \(I_{on}/I_{off}\) ratio and on-state resistance \((R_{on})\), with operating temperature is also lower in ESDG MOSFET in comparison to DG, ESS and bulk MOSFET.
6.7 Digital Performance

CMOS inverter circuit is widely used in microprocessor, SRAM, and other digital logic circuits. It is also used to construct several analog circuits such as image sensors, data converter and densely integrated circuit for many types of communication systems. Hence, it is very important to get good static as well as dynamic performance for the device. In this section, digital performance of ESDG, DG and ESS MOSFETs has been compared using static (Voltage Transfer Characteristics and noise margin) and dynamic (transient analysis) performance of CMOS inverter which is the basic building block for digital circuit design. CMOS inverter is constructed using N-MOS (pull-down MOSFET) as a driver and P-MOS (pull-up MOSFET) as a load [Mitra04] [Buddharaju07] [Taur09] [Weste09] discussed in detail in chapter 4 for single gate geometry MOSFETs.

6.7.1 Static Performance

In CMOS inverter circuit, in order to have high-to-low transition in the voltage transfer curve to occur close to the mid-point, it is compulsory that, $I_p$ (P-MOS current) and $I_n$ (N-MOS current) are matched with each other. In this chapter, threshold voltage adjustment is achieved by changing the metal gate work-function of P-MOS and N-MOS transistor. Ideally power dissipation is zero in CMOS inverter because the complementary CMOS gates drawn zero current. However, in real devices power dissipation is not zero due to sub-threshold leakage between source and drain region.

Figure 6.13 illustrates the Voltage Transfer Characteristics (VTC) of CMOS inverter based on three different devices. Results reflect that, DG MOSFET exhibits good high-to-low transition as compared to bulk ESS MOSFET due to lower sub-threshold slope of the device. Further improvement in Voltage Transfer Characteristics is observed by using empty space layer in between the channel of DG MOSFET i.e. ESDG MOSFET. This is only because of the reduction in sub-threshold slope and enhancement in device gain in ESDG MOSFET as compared to DG and single gate ESS MOSFET.
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The change in input voltage $\Delta V_{in}$ at which the output voltage falls from 90% to 10% of the output voltage ($V_{in} @ V_{out} (90\%) - V_{in} @ V_{out} (10\%)$) is 20 mV (i.e. transition region) in ESDG MOSFET however it is 50 mV in DG followed by 0.14V in ESS MOSFET. Noise margin ($NM$) in the digital circuit determines the maximum allowable noise voltage on the input of the gate so that the output is not corrupted [Hauser93] and is measured by the size of the maximum square that can fit itself and its complementary curve discussed in detail in chapter 4. Figure 6.13 also shows that the noise margin of ESDG MOSFET is 45% higher than ESS MOSFET and 14% higher than the DG MOSFET due to enhanced vertical coupling between upper and lower gate and suppression in the lateral coupling (i.e. fringing field lines) from drain to source through empty space layer. This implies that ESDG MOSFET is less influenced by the noise present at the input of the circuit as compared to other devices.

6.7.2 Dynamic Performance

The dynamic response of inverter is useful to compute the propagation delay of the inverter circuit and hence the speed of the circuit. Lesser the propagation delay, higher is the speed of the circuit. The dynamic performance of the inverter circuit also depends on the internal nodal capacitances such as gate to drain capacitance ($C_{gs}$),

Figure 6.13 Voltage Transfer Characteristics of CMOS inverter circuit using P-MOS as load and N-MOS as a driver MOSFET; $L=60$ nm, $C_L=1$ fF, $t_{si}=25$ nm, $t_{ox}=1.7$ nm, $t_{box}=10$ nm, $V_{dd}=0.5$ V and $W=325$ nm [Kumari13b].
gate to source capacitance \( (C_{gs}) \) in single gate geometry and \( C_{gs}, C_{gd} \) and gate to gate capacitance in double gate geometry. Thus, the frequency and gate bias dependence of total parasitic capacitances (i.e. \( C_{gg} \)) of ESGD, DG, ESS and bulk MOSFET is plotted in figure 6.14 (a) and (b) respectively.

Figure 6.14 Variation of (a) parasitic Capacitance \( (C_{gg}) \) with operating frequency (above ZTC Point) at different temperature for \( V_{gs}=1.0 \, \text{V} \). (b) total Capacitance with gate to source voltage \( (V_{gs}) \); \( V_{ds}=0.5 \, \text{V}, L=60 \, \text{nm}, t_{si}=25 \, \text{nm}, t_{ox}=1.7 \, \text{nm}, W=325 \, \text{nm} \) and \( t_{box}=10 \, \text{nm} \) [Kumari13b].

In depletion region the total gate capacitance comprises of three components i.e. 1) gate to source capacitance \( (C_{gs}) \), 2) gate to drain capacitance \( (C_{gd}) \) and 3) gate to bulk capacitance \( C_{gb} \) in bulk MOSFET or gate to gate capacitance \( C_{gg} \) in double gate MOSFET. However, in strong inversion region, \( C_{gg} \) in double gate or \( C_{gb} \) in bulk MOSFET are approximately equal to gate oxide capacitance \( (C_{ox}) \) which depends only on the gate oxide thickness and permittivity of the oxide material. Since parasitic capacitances, namely \( C_{gs} \) and \( C_{gd} \) are important parameters for analog/RF and digital applications, it is necessary to extract these components [Kaur07c] [Chaujar10].

In ESDG MOSFET, the effective source or drain diffusion area decreases, thereby showing reduction (slightly \( \sim 10\% \)) in \( C_{gg} \). Thus the actual contribution of the buried oxide layer in ESDG is to suppress the effect of parasitic capacitances. ESS MOSFET exhibits lower parasitic capacitances as compared to bulk MOSFET due the presence...
of buried oxide layer in the channel region. DG MOSFET also exhibits higher parasitic capacitances in comparison to bulk. Due to the presence of ESS layer in the channel region of ESDG MOSFET, lower parasitic capacitances are achieved in ESDG MOSFET as compared to DG MOSFET. As the operating temperature increases, total capacitance of the different device decreases.

Figure 6.15 (a)-(c) illustrates the impact of load capacitance \( (C_L) \) on the transient behavior of ESDG, DG and ESS MOSFET based CMOS inverter respectively. As the load capacitance \( (C_L) \) increases, overshoot voltage decreases, however this also increases the propagation delay of the circuit and hence degrade the circuit performance.

**Figure 6.15** Transient analysis of CMOS inverter based on different devices (a) ESDG MOSFET (b) DG MOSFET and (c) ESS MOSFET at different load capacitance \( (C_L) \); remaining parameters are: \( V_{dd}=0.5 \) V, \( L=60 \) nm, \( t_{ox}=25 \) nm, \( t_{si}=1.7 \) nm, \( W=325 \) nm and \( t_{box}=10 \) nm [Kumari13b].
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Propagation delay is calculated by taking average of fall time and rise time of output response and is given by:

$$\tau_d = \frac{(t_{pHL} + t_{pLH})}{2}$$  \hspace{1cm} (6.16)

Where the rise time \((t_{pLH})\) of the inverter is defined by the time taken for a waveform to rise from 10% to 90% of its steady state value and similarly fall time \((t_{pHL})\) is defined as the time taken for a waveform to fall from 90% to 10% of its steady state value [Weste06] [Li09] [Patil11].

The estimated propagation delay is maximum in ESS (42 ps) MOSFET followed by DG (11.2 ps) and ESDG MOSFET (5.3 ps). The reduction in delay in ESDG MOSFET is attributed to lower sub-threshold slope, higher device gain and lower parasitic capacitance as compared to other devices. In addition, impact of \(C_L\) variation, on propagation delay is also lesser in ESDG MOSFET followed by DG and ESS MOSFETs.

6.7.3 Logic Gates (NAND and NOR Gate)

The most fundamental building blocks of digital circuits are CMOS inverter along with the NAND and NOR logic gates [Mitra04]. The performance of inverter has been discussed above. In this section, application of ESDG MOSFET has been extended to study the behavior of logic gates and is also compared with other devices. Figure 6.16 and figure 6.17 shows timing diagram of NAND and NOR logic gate respectively based on different devices. It is evident from the figure that ESDG MOSFET exhibits better circuit performance as compared to DG and ESS MOSFETs.

The estimated propagation delay in NAND gate calculated from the slope of the transition region of the logic gates is 8 ps for ESDG MOSFET, 12 ps for DG MOSFET and 18 ps for ESS MOSFET. The propagation delay in case of NOR gate is 8 ps for ESDG MOSFET, 11 ps for DG MOSFET and 22 ps for ESS MOSFET.

The superior performance of ESDG MOSFET is due to the 1) higher output resistance attributed to lower CLM effect in the device 2) higher device gain due to the higher \(R_{out}\) and 3) higher trans-conductance of the device.
Figure 6.16 Timing diagram of NAND Gate based on different devices at room temperature; $V_{dd}=0.5$ V, $L=60$ nm, $t_{si}=25$ nm, $t_{ox}=1.7$ nm, $W=325$ nm and $t_{box}=10$ nm [Kumari13b].

Figure 6.17 Timing diagram of NOR Gate based on different devices at room temperature; $V_{dd}=0.5$ V, $L=60$ nm, $t_{si}=25$ nm, $t_{ox}=1.7$ nm, $W=325$ nm and $t_{box}=10$ nm [Kumari13b].
The other factors which may also affect the rising time of the logic gate circuits are on state resistance. Since the on-state resistance $R_{on}$ of the ESDG MOSFET is lower as compared to the DG MOSFET. Thus the charging and discharging time of ESDG MOSFET based logic circuit through external load capacitor is lower as compared to the DG MOSFET.

### 6.7.4 Three Stage Ring Oscillator

In this section, the output response of the different devices based ring oscillator has been investigated. Ring oscillator is represented by the odd numbers of the series combination of the inverter circuit generally used to synchronize the operations in digital electronic system discussed in detail in chapter 4.

The frequency of oscillation ($F_o$) of the ring oscillator is given by:

$$F_o = \frac{1}{2\pi\tau}$$

where $\tau$ is delay of the oscillator and $n$ is the no of inverter circuit connected in series [Mandal10]. Lower the delay, higher will be the frequency of oscillation. In the present analysis $n$ is taken as 3.

![Timing diagram of 3-stage ring oscillator based on different devices at room temperature](image)

*Figure 6.18* Timing diagram of 3-stage ring oscillator based on different devices at room temperature; $V_{dd}=0.5$ V, $L=60$ nm, $t_{si}=25$ nm, $t_{ox}=1.7$ nm, $W=325$ nm and $t_{box}=10$ nm [Kumari13b].
Figure 6.18 shows the timing diagram of 3-stage ring oscillator using different devices. The calculated propagation delay is lower for ESDG MOSFET i.e., 7 ps while it is 17 ps for DG and 25 ps for ESS MOSFET thereby showing higher frequency of oscillation as compared to DG and ESS MOSFETs. This is because of the ultra thin body of the ESDG MOSFET that confines the electric field and charges in channel region leading to additional advantage of reduced parasitic capacitances. The higher frequency of oscillation in ESDG is attributed due to the a) lower sub-threshold slope ($S$) b) higher device gain ($g_{md}/g_d$) and c) higher output resistance ($R_{out}$) as compared to ESS and DG MOSFET. Thus ESDG based ring oscillator can be used more efficiently as part of a PLL for clock and for data recovery and thus extended the usability of the device beyond the conventional devices for digital applications.

6.8 Summary

This chapter presents the complete drain current model from sub-threshold to saturation region incorporating velocity saturation and DIBL effects for undoped symmetric ESDG MOSFET using Evanescent Mode Analysis and the results obtained are well matched with the simulation results. The reduction in the threshold voltage roll-off with channel length is the indication of the improved scaling capability of the ESDG MOSFET. The analog and digital performance of ESDG MOSFET is also compared with conventional DG, bulk ESS and bulk MOSFET. Enhancement in early voltage ($V_{ea}$) and output resistance ($R_{out}$) in ESDG MOSFET can be achieved because of the enhanced drain current and highly suppressed drain-conductance. This implies that, ESDG MOSFET is more immune to SCEs in terms of lower DIBL, sub-threshold slope and off-state current. ESDG MOSFET has higher noise margin as compared to ESS and DG MOSFET thereby showing distortion less output. The delay of the ESDG MOSFET is also lower than DG and ESS MOSFETs, thereby showing immense potential for high speed digital applications. The other figure of merits needed for high speed digital applications like higher $I_{on}/I_{off}$ ratio, higher device gain ($g_{md}/g_d$), smaller sub-threshold slope ($S$) and lower on-state resistance ($R_{on}$) are also improved by using ESDG MOSFET in comparison to DG and ESS MOSFETs.
ESDG MOSFET is also less sensitive to temperature variation (in terms of drain current, trans-conductance, device gain, output resistance and early voltage) as compared to others devices. Therefore the improved short channel immunity and reduced leakage current of ESDG MOSFET at higher operating temperature make it a potential candidate for analog and fast digital applications in near future.
6.9 References


[Chung07] T.M. Chung, B. Olbrechts, U. Södervall, S. Bengtsson, D. Flandre, J.-P. Raskin “Planar double gate SOI MOS devices: fabrication by...


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