ABSTRACT

In recent years, as a result of advancing VLSI technology, Orthogonal Frequency Division Multiplexing (OFDM) has received a great deal of attention and has been adopted in many new generation wideband data communication systems such as IEEE 802.11a, IEEE 802.16e, HiPerLAN/2, Digital Audio/Video Broadcasting (DAB/DVB), and for 4G Radio mobile communications. This is because of its high bandwidth efficiency as the use of orthogonal waveforms with overlapping spectra. The immunity to multipath fading channel and the capability for parallel signal processing make it a promising candidate for the next generation mobile communication systems. The modulation and demodulation of OFDM based communication systems can be efficiently implemented with an FFT and IFFT, which has made the FFT valuable for those communication systems. The complexity of an OFDM system highly depends upon the computation of Fast Fourier Transform (FFT) algorithm. We also present experimental results and analysis regarding dynamic reconfiguration.

Since deriving an efficient OFDM is still in the research phase, so far there is no prescribed design procedure for FFT to be used in OFDM design. The FFT processor has not been paid attention to very much in the past, because of the hardware complexity of FFT processor. At present some of the standards are using fixed Radix-4 FFT Algorithm. This thesis addresses the problem of deriving an efficient FFT processor and its application is studied in OFDM system.

In the mobile communication systems the different standards mentioned above have different demands in the length of FFT/IFFT. The Mixed-Radix FFT algorithm is based on sub-transform modules with highly optimized small length FFT which are combined to create large FFT. This adds a bit of complexity to the algorithm compared to radix-r, but in return it gives more options in choosing the transform length.
In this work, several FFT algorithms such as fixed radix-2, radix-4, split radix and proposed mixed radix 4-2, R2MDC and modified R2MDC were designed and modeled using VLSI design process and their performance was analyzed. Also the existing OFDM system has been tested with these FFT algorithms and their performance was analyzed with respect to occupation of Area in FPGA and Power. The results show that OFDM with proposed Modified R2MDC FFT architecture design can efficiently save the area and power, which may be attractive for future mobile communication systems. Also these VHDL simulation results have been tested practically by implementing in the Altera DE-2 FPGA development board.

Recently, various FFT algorithms have been proposed to meet real-time processing requirements and to reduce hardware complexity over the last decades. Since the pipeline FFT algorithms are well suited for digital signal processing applications where high-speed data throughput is the dominant requirement, several pipeline FFT algorithms have been proposed. Pipelining is a standard way of decomposing an operation into concurrently operating stages to increase throughput at a moderate increase in area. A wide variety of applications such as digital filters, video compression and general-purpose microprocessors may be decomposed into pipeline structures. Pipelines can be implemented both synchronously and asynchronously. Among these algorithms, the Radix-2 FFT algorithm derived by index decomposition technique. It has the same multiplicative complexity as Radix-4 algorithms, but still retains the radix-2 butterfly structures. However, the Split-Radix algorithm has the disadvantage of irregular structure which is not easily implemented in the hardware viewpoint. The Mixed-Radix FFT algorithm is based on sub-transform modules with highly optimized small length FFT which are combined to create large FFT.

First, Radix-2, Radix-4 and the Efficient Mixed Radix 4-2 Butterfly FFT with bit reversal for the output sequences derived by index decomposition technique is designed to FFT/IFFT processor for wireless communication, and its application is studied in existing OFDM systems.
Second, the baseline MIMO-OFDM system uses the same number of fast Fourier transform (FFT) blocks as antennas. Then, MIMO-OFDM could be extended from OFDM. The implementation of OFDM was necessary for comparing its performance with that of MIMO-OFDM. The implementation efficiency of our pipelined architecture, compared with the baseline MIMO-OFDM system, is evaluated using two methods: (1) using just one FFT block, and (2) using Radix-2 Pipelined streaming FFT block, versus a Radix-4 FFT block used in the baseline MIMO-OFDM system. The implemented optimized MIMO-OFDM with our pipelined structure, which reduced the amount of resources and satisfied the requirements of 802.11a WLAN.

Finally, a novel method is proposed that can be extension of Radix-2 architecture and it can be called as MOD-R2MDC FFT; the proposed MOD-R2MDC architecture is implemented in FPGA, then the performance of various 64 point FFT such as Radix-2, Radix-4, split Radix, mixed -radix 4-2, R2MDC and the proposed modified R2MDC were carried out and their performance were analyzed with respect to the number of CLB slices, utilization factor and Power consumption. it was observed that the proposed Modified R2MDC is used least numbers of CLB slices when compared to other FFTs and taken less power than the existing radix-2 and existing R2MDC algorithms and shows that it can be used for low power applications such as MIMO-OFDM system.