CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

In this thesis, two new efficient frameworks for DBA in next generation access networks are proposed - one for EPON-WiMAX integrated network and another for EPON-LTE converged network. The proposals are implemented and tested against the conventional scheme using OPNET Modeler.

The DDA-EPON algorithm reduces the load on the OLT by sharing the work of DBA estimation between the OLT and ONU thereby reducing the delay and improving the bandwidth utilization of the integrated architecture. From the observation of the WiMAX-EPON integrated architecture, it is proved that the proposed architecture is better than the existing scheme in terms of:

- Throughput – the processor requires less clock cycles to run the DDA-EPON algorithm than the conventional algorithm. It could also be inferred that neither the OLT nor the ONU is overloaded due to the modifications, and hence provides provisions for increasing the number of ONUs that could be supported by an OLT.

- Service classes – there is an improvement in the throughput of the UGS scheme and is an appreciable improvement since it is not achieved at the expense of reducing throughput of other service schemes.
• Voice – voice packet end to end packet delay has significantly reduced while maintaining the jitter of voice.
• Video – traffic received for video packets has improved.

The results show that the percentage of utilization has almost halved, and hence for the same set of hardware the number of ONUs supported by an OLT could be doubled.

The CDA-EPON algorithm improves the DBA process by enhancing QoS by favoring high priority requirements than low priority requirements and also establishes fairness in the process among the high priority ONUs by serving in a round-robin process. Observations from the EPON-LTE architecture reveal that:

• The performance of the network has significantly increased along with ensuring QoS in the network.
• Also, the system proves to be an efficient high capacity backhaul network with the fact that the measured delays for all services are well within the limits defined by the LTE standard.

Both the proposed architectures are tested for hardware compatibility by implementing and evaluating the performance in network processor. Observations prove that both these architectures do not consume more clock cycles than the existing architecture, thereby validating the effectiveness of the architectures.

7.2 FUTURE SCOPE FOR RESEARCH

It would be interesting to see how the proposed architectures combine with existing setup. Also, it would be even more interesting to evaluate the proposed framework in a real time Switch.
Both the proposed architectures are tested using networks with stochastic or random process models. It would be interesting to evaluate the system using deterministic models. Deterministic simulations have known input set and result in a unique set of outputs. Since max and min values are defined, the parameters occupy a defined space. The model represents reality and is easier to build and interpret than a stochastic model. However, large numbers of inputs and outputs make such models extremely complicated and multiple sets of inputs can result in fixed single set of outputs.