CHAPTER 6

CONCLUSION

6.1 SUMMARY OF THE THESIS

The problem of test pattern generation for multiple stuck-at faults in VLSI circuits is a challenging task because of the large complexity involved. This complexity is due to the huge amount of data involved in this process to store the results of simulation of these faults. Also for a circuit involving ‘n’ lines there are around $3^n - 1$ multiple stuck-at faults as compared to $2n$ single stuck-at faults.

In this research work, four methodologies have been proposed. Three of them were proposed for test pattern generation for multiple stuck-at faults and one for the test power reduction.

Test pattern generation has been carried out first using evolutionary algorithms like GA and MPSO. As the patterns have to be generated from a large search space, GA and MPSO were chosen. In MPSO, the average CPU execution time was found to be lesser than that obtained using GA. The switching activity due to the transitions between the test patterns was also found to be less in the case of MPSO than that obtained due to GA. This is because in MPSO, while generating the test patterns itself, the transitions between successive patterns were kept at a minimum. Hence an average reduction of 58.54 in ASA was obtained when compared to GA.
The next method of test pattern generation was done using ZBDDs. This method generated test patterns which were incompletely specified than that by earlier proposed methods. Hence the test patterns consisted of 0s, 1s and don’t-cares.

For test power reduction, two techniques were used namely the reordering technique and don’t-care filling technique.

As the average switching activity was found to be less in MPSO, a reordering technique was used to reorder the test patterns obtained using MPSO to further reduce the test power.

Reordering was done based on a distance metric between the test patterns applied as inputs to the circuit and also based on the internal switching of nodes inside the circuit. Various distance metrics like Hamming, Euclidean and Tversky were analyzed and it was found that Tversky distance gave better results.

A second method of test power reduction was proposed using a don’t-care filling technique. The test patterns generated using ZBDD were incompletely specified and hence suitable don’t-care filling techniques like 0-fill, 1-fill, adjacent-fill and Minimum Transition fill (MT-fill) techniques were employed to fill the don’t-care in test patterns. It was found that the MT-fill technique had the minimum number of transitions when compared to other fill techniques and an average ASA reduction of 217.3 when compared to the MPSO technique and an average ASA reduction of 275.9 when compared to the GA technique was obtained.

Thus it is concluded from the report of the research work carried out that the ZBDD based method of test pattern generation along with minimum-transition-fill technique is one of the best solutions for generation
of test patterns for multiple stuck-at faults with reduced test power. Reordering of test patterns will not have any impact on the faults because the order in which these patterns are used to test the circuit is immaterial as far as the faults are concerned.

6.1 SUGGESTIONS FOR FUTURE WORK

The faults considered for research work were only stuck-at faults. However, other faults like multiple bridging, multiple delays or multiple stuck-open can be modeled and test patterns can be suitably generated. Further a combination of these faults also can be modeled and test patterns can be generated. Also, if reordering had been applied to the incompletely specified test patterns, further reduction could be obtained.