CHAPTER 7

CONCLUSION AND SCOPE FOR FUTURE WORK

7.1 CONCLUSION

This research work is focused on reversible logic based circuit design. It is shown that proposed work is efficient in terms of garbage outputs, constant inputs, logical complexity, device utilization, power consumption and delay. The various combinational circuits have been designed using proposed NTG and corresponding comparison is made with respect to Rgate logic. The various sequential circuits have also been designed; it has been shown that the proposed designs have 5% higher speed and 10% less power when compared to the conventional design styles. Based on the input bit pattern and complexity requirement for the design which enables to use n-bit input, the reversible logic design can be used for any kind of circuit. For instance a single reversible gate acts as a full adder along with other three outputs that can be utilized further thus the maximum combinational path also reduces. This idea is utilized for high speed designs. In the reversible logic based barrel shifter the logical state of the computational device before the operation of the device can be determined by its state after the operation i.e., the input of the system can be retrieved from the output obtained from it which is helpful in reducing switching activity i.e. the computation made for the particular gate is used instead of changing the values with input. The new computational architecture still preserves the high degrees of simplicity, regularity and concurrency.

In this research work, various multiplier architectures are designed and implemented. Various add and shift multiplier circuits are implemented using proposed logic and necessary comparison is made. The results show that the CSD multiplier has 11% less delay and 10% power improvement when compared to
conventional CSD multiplier design. The digital FIR filter is designed where adders and multipliers used are based on proposed reversible logic design. FIR filter using wallace tree multiplier based on proposed NTG logic provides 10% reduced delay as compared to FIR filter design using array multiplier; also it has 17% improvement in power consumption. The digital FIR filter designed using multiplexer based proposed scheme offers almost 40% reduction in hardware resources. The proposed work forms an important step in the building of complex logic circuits for quantum computers. In coming years, reversible logic as quantum software and desktop quantum computer can be a challenge to young scientists. The circuits with information loss only as power consumption can be replaced by reversible logic based designs in coming future; hence reversible logic will be promising in achieving almost zero power consumption. Reversible logic offers performance advantages over conventional technology, but faces a long and expensive technology development path.

7.2 SUGGESTIONS FOR FUTURE WORK

As such, there are still many challenges before actually turning reversible logic into a practical competitive technology. Due to irreversible gates, the power loss is negligible for current logic technologies using adiabatic design. A major limitation for the today’s CMOS technology is represented by increased heat dissipation of the silicon chips. Therefore, reversible circuits present the promise of very low power computation. In addition, reversible logic synthesis has a close relation with quantum logic synthesis, and the method of reversible logic synthesis can be used to implement quantum logic synthesis. Thus, the study of reversible logic synthesis will contribute to the progresses in the related research fields, including design of the ultra-low power IC and quantum computing. The proposed method will have broad applications in hardware implementations of many DSP algorithms. The CSD method can be used efficiently in color transforms for processing of images. Using CSD representation of reversible color transform coefficients and exploitation of their common sub expressions reduces the complexity of the hardware implementation significantly. The proposed structure is capable of implementing multipliers in filters, i.e. by taking advantage of the CSD
representation, the efficient FIR filters could be designed with presently available
CSD FIR filter approaches. The CSD FIR filters can be implemented for high
performance MPEG filters for images.

Future work related to building of the proposed reversible logic by using
technologies such as CMOS, in particular adiabatic CMOS, optical, thermodynamic
technology, nanotechnology and DNA technology is another important aspect. The
proposed method will have broad applications in hardware implementations of many
DSP algorithms. The proposed structure is capable of implementing multipliers
using add and shift method, i.e. by taking advantage of reversible barrel shifter, the
efficient multipliers can be designed which could be better than presently available
approaches. An interesting future work could be to develop efficient reversible
counters and barrel shifter circuits and further it could be advantageous to design an
arithmetic and logic unit. Reversible logic contributes to the progresses in the related
research fields, including design of the low power and high speed devices. A
promising way to secure funding for the required technology development would be
to join forces with a high priority problem that can be solved by computers but
exceeds the limits of conventional technology.