CHAPTER 7

CONCLUSION

7.1 CONCLUSION

This thesis represents the research work of developing new approaches for implementing Viterbi decoder designs to minimize computation memory, power consumption, BER and latency. This work examines the decoding process of the Viterbi algorithm, the architecture of the Viterbi decoder, and the implementations of the basic functions. This enables the design problems to be discovered. Then a variety of design techniques are described and applied to the decoder design to improve its efficiency aspects. Simulations on both software and hardware test the new designs. The results give a clear view of the improvement of the modifications and enable a novel general methodology for significantly reducing complexity of decoding convolutional codes to be proposed.

A non-polynomial approach to achieve a high throughput with low bit error probability Viterbi decoder is proposed and implemented. Low Bit Error Rate (BER) can be achieved by increasing the $d_{\text{free}}$ distance of the viterbi decoder without increasing size of the decoder architecture. The increase in $d_{\text{free}}$ has been achieved by using non-polynomial convolutional coding method. The performance of Viterbi decoder with the proposed method has been improved in such a way that 75% of errors will be detected and corrected. An experimental result shows that the proposed viterbi decoder provides satisfactory probability of error ($P_b$) performance and high operating
speed under various conditions including AWGN, co-channel interference and adjacent channel interference environments.

The next focus of the research in the low-power design of Viterbi decoders at logic level is reduction of dynamic power dissipation in the standard cell design environment. We have investigated power dissipations of three different implementations of Viterbi decoders: the shift update, selective with clock gating and toggle filtering and deep pipelined with all the above low power techniques Viterbi decoder Scheme. We have proposed a low power Viterbi decoder design based on the traceback approach. The schemes employed for our low-power design are clock gating of the survivor path storage block and toggle filtering of output generation block. We have implemented the three designs in the standard cell design environment and measured the performance in terms of area and power dissipation. Among the three implementations, it is observed that the proposed low-power design takes the smallest area and dissipates the least power. The proposed design reduces the power dissipation of the register-exchange approach by 68.82%. Finally, it is difficult to make a head-to-head comparison of power efficiency between the proposed method and other existing methods due to different environments (such as hard decision versus soft decision) and constraints imposed.

The thread parameter of our design is memory management (utilization) in Viterbi decoder. A novel Zig-Zag algorithm for survivor memory management in Viterbi Decoders is proposed and implemented. This method utilized only one RAM block for the survivor memory unit as well as trace backs decoding process. We achieved a latency of 50% compared to 100% for the trace back algorithm. Only 56.09% of total memory has been utilized in the proposed algorithm than the trace back method. Total delay is only 6.785ns but it is 12.013ns for the trace back algorithm approach.
The speed and throughput of the Viterbi decoder is improved by implementing deep pipelining method. The Add-Compare-Select (ACS) and Trace Back (TB) units and its sub circuits of the decoder have been operated in deep-pipelined manner to achieve high transmission rate. The advantages of using deep-pipelined architecture are: low area, high throughput, and high speed. The speed of the decoder can be improved by applying pipelining approach to ACS and TBU. The whole decoder works on pipelining principle in which the sub blocks also perform pipelining operation up to the trace back depth. With the use of the 0.22µm processes, high-speed operations exceeding 145 Mega symbols per second are achieved.

7.2 FUTURE WORK

According to information theory, to achieve high channel capacity requires more redundancy or more complex computation to maximize code word distances of the codes. However, the theory does not suggest that the decoding process should also be more complex. Therefore, it is necessary to analyze the relationship of channel capacity and decoding complexity. So that the optimum codes can be discovered in terms of both BER performance and decoding complexity.

Since the maximum likelihood decoding process could be viewed as the classic optimization problem, it can also be solved using the Hopfield neuron networks. By properly defining the energy function of the code words path distance, the most likely path can be identified by the revolving of the neuron network.

The ideal of using pre-decoded data from the zero Hamming distance path is decoder independent. Therefore, it could be adopted in other convolutional decoding applications, e.g. Turbo decoder, to minimize power consumption.