Abstract
Over the last couple of decades architecture of 51 family core is preferred for the most of the embedded design, apart from 51 family - AVR and Microchip PIC are known and popular chips in the world of embedded system, however in last decade ARM core has emerged as a viable alternative for embedded design. ARM architecture offers superior performance in terms of power efficiency, data processing, throughput and above all effective load/store architecture of RISC.
This thesis presents performance enhancement of ARM architecture – architecture design and enhancement concerns lot many issues, I have focused on power consumption, branch prediction logic. Thesis presenting the overview of different ways for effective power reduction mechanism particularly for embedded systems. Propose “backward taken forward not taken (BTFNT)” algorithm for the branch prediction using simplescalar toolset simulator. Algorithm developed in simplescalar toolset support ARM instruction set architecture and many others like X86, SPARC etc. The proposed thesis describes the enhancement of ARM7/ARM7TDMI architecture by embedding free RTOS on it. Throughput of the system can be increased by parallelism either of process level, data level or instruction level parallelism. Process (Thread) level parallelism realized by Multitasking of four tasks in ARM7 core with the help of RTOS.
ARM cortex- M core is enhanced for mixed signal processing using the CyPress PSoC device for obtaining better performance in terms of power consumption and effectiveness of addition or removal of analog and digital blocks as per the custom design requirement. Real time monitoring & data logging system is employed with ARM core is presented in the second part of the thesis.
Last part of the thesis presents enhancement of ARM11 core by porting of an open source operating system on it. A single credit card size board with ARM core can be effectively utilized as complex independent computing machine, with most of the desktop facility and the same core is being utilized for real time monitoring and data logging using additional interface.