Chapter 5

Introduction ARM Cortex series

5.1 ARM Cortex series variants
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5.1 ARM Cortex Series Variants:

ARM architecture has evolved over the time and ARM core also available in latest cortex[2] Series, again to reuse the term A R M, Cortex Series comes in three different profiles as listed below.

1. ARM Cortex – A series
2. ARM Cortex – R series
3. ARM Cortex – M series

5.2 ARM Cortex – A Series:

Cortex – A series provides varieties of application processors and it offers solution for the devices having strong operating systems and user applications[2] consisting of low-cost-handset in case of smart phones, mobile computing platform, digital TV and set top box.

Important feature[2] of Cortex – A series

- High performance – Cortex A devices offers power efficient performance for the targeted applications. It can be realized in mobile smart phone, tablet devices and wireless infrastructure applications
- Best suited for accessing internet through mobile – supports Adobe flash, consists of high performance NEON Engine for broad support of media codec and low power consumption allows continuous browsing.
- Supports Multicore Technology – single to quad core is being utilized for performance oriented applications. Provides coherency throughout the processor for memory and peripheral access with the help of Accelerator Coherency Port (ACP).

5.2.1 Cortex – A Series Variants:

Cortex – A series available with different variants[2] for varieties of applications

- Cortex – A5 Processor
- Cortex – A7 Processor
- Cortex – A8 Processor
- Cortex – A9 Processor
Cortex – A12 Processor
Cortex – A15 Processor
Cortex – A50 series Processor

Basic application processor Cortex – A5 architecture[2] is shown in Figure 5.1. The Architecture is based on version 7. Important features of the architecture are – it is a multicore architecture, comprises of Instruction & data cache separately, NEON data engine for media codec and floating point unit.

Figure 5.1 ARM Cortex A5 Architecture

As far as the various other application processors concern they are having advance features based on the application need. Pipelining scheme of Cortex-A7[2] is shown in Figure 5.2 and Figure 5.3 shows the pipeline scheme[2] of cortex – A15. This pipeline architecture comprises of integer, multiply, floating point, load/store dimensions with writeback option.

Figure 5.2 ARM Cortex A7 Pipeline
5.3 ARM Cortex – R Series:

Cortex – R series consists of Real Time Processors which offers[2] high-performance computing solution, very good fault tolerance, detect errors thereby maintain reliable system operation and real time response for embedded systems.

Important features[2] of Cortex – A series:

- High-Performance – for executing complex code at rapid rate with DSP functionality. High clock frequency, deeply pipelined microarchitecture. Dual core multi processing configuration. Hardware SIMD instructions for DSP and Media.
- Performance enhancing technologies – instructions are pre-fetch, branch prediction and superscalar execution. Inclusion of Floating Point Unit (FPU).
- Truly real time - in terms of response of interrupt and accessing information to/from memories. Fast, bounded and deterministic interrupt response. Tightly Coupled Memories (TCM) for faster access. Low Latency Interrupt Mode (LLIM) to accelerate interrupts entry.
- Harvard architecture with instruction and data cache controller.
- Highly secure and safe - User and privilege software operating modes. Memory protection unit.
- High performance AMBA-AXI bus interface.
- Cost effective

### 5.3.1 Cortex – R Series Variants:

Cortex – R profile available in different variants[2] in real time processors

- Cortex – R4 processor
- Cortex – R5 processor
- Cortex – R7 processor

![Figure 5.4 Cortex - R4 Processor Architecture](image)

**Figure 5.4 Cortex - R4 Processor Architecture**

Figure 5.4 shows Cortex – R4 processor Architecture[2] – which is said to be the basic architecture in real time processor series. It comprises of version 7 of ARM core CPU, along with that it is also having two Tightly Coupled Memory modules, separate data and instruction cache controller, memory protection unit and Floating point unit. All these modules are communicating with the help of high performance AMBA – AXI bus interface.

Cortex – R5 architecture comes with enhancement like dual core and high priority low latency peripheral port (LLPP) along with that it also has Accelerator Coherency port (ACP). Cortex – R7 architecture introduce new technology including out-of-order instruction execution and dynamic register re-naming.
5.4 ARM Cortex – M Series:

Cortex – M series consists of Microcontroller based processors[2] having energy efficient upward compatible processor, code reuse facility and better connectivity.

Important features[2] of Cortex – M series:

- **Energy Efficient** – Operates at lower MHz and/or with shorter activity period. Sleep mode is available in architecture which is better than that of 8/16 bit. Reduce energy cost and improves battery life.
- **Small code size** – dense instruction set, requires small size of ROM, RAM and FLASH. Performance per byte is more than that of 8/16 bit devices. Reduces silicon cost.
- **Easy to use** – standardize platform across all the vendors, provides good code compatibility. Unified tools and OS support. Software development is fast and reusable.
- **High performance** – gives better throughput for given operating frequency compared to all 8/16 bit devices.

5.4.1 Cortex – M Series Variants:


- Cortex – M0 Processor
- Cortex – M0+ Processor
- Cortex – M1 Processor
- Cortex – M3 Processor
- Cortex – M4 Processor

Cortex – M series processor comprises state of the art technology which delivers best performance, apart from above listed important feature Cortex – M series controller has got Nested Interrupt Vector Controller (NVIC) as an integral part of the processor. Table 5.1 describes the support of NVIC[2].

<table>
<thead>
<tr>
<th>Processor</th>
<th>No. of IRQ</th>
<th>NMI</th>
<th>System exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex – M0,M0+, M1</td>
<td>32</td>
<td>1</td>
<td>Yes</td>
</tr>
<tr>
<td>Cortex – M3, M4</td>
<td>240</td>
<td>1</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 5.1 NVIC Support For Cortex M Series Processor
Basic architecture of Cortex – M0 processor[2] is shown in Figure 5.5 which comprises the NVIC module as an integral part of it. Figure 5.6 shows the working of NVIC with Cortex – M series processor[2]. NVIC deals with IRQs, NMI and System exceptions.

Figure 5.5 Architecture Of Cortex - M0 Processor

Figure 5.6 NVIC Working in Cortex M series Processor
As far as M0 and M0+ is concerned both are almost identical in architecture except few changes in M0+. In Cortex – M0 we have 3 - stage pipeline whereas in M0+ it has been reduced to 2 - stage pipeline which lowers the power consumption. On the other side M0+ has got better debug option with the help of Micro Trace Buffer (MTB) by which it is easier to trace any instruction. Following Figure 5.7 shows the progressive graph[2][22] of Cortex – M series variant with respect to performance, cost and integration.

Figure 5.7 Cortex - M Series Performance Chart

Figure 5.8 Cortex - M3 Processor Architecture
Figure 5.8 shows the architecture of Cortex – M3 processor[2] which is having enhanced features like 3 – stage pipeline with branch speculation and memory protection unit. Large number of physical interrupts up to 240 maximum. Along with conventional interrupt it has also the support of Non-Maskable Interrupt (NMI). As far as instructions are concern it fully supports Thumb and Thumb2 modes. Instruction set[2] for Cortex – M0 and M3 is shown in Figure 5.9.

![Instruction Set For Cortex - M0 and M3](image)

5.5 Comparison Of Cortex – M Series With 8/16 bit MCU:

There are various aspects on which ARM Cortex – M series is superior over the conventional 8/16 bit MCU like 51 family, PIC and MSP430.

- **Code Size of Cortex M 32 bit versus 8/16 bit MCUs:**
  - Instruction size of 8 bit MCU[22][23]
    - For 8051 it is from 8 bits to 24 bits
    - For PIC16 it is 16 bits
    - For PIC18 it is 18 bits

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Instruction size of 16 bit MCU

- For PIC24 it is 24 bits
- For MSP430 can be upto 32 bits for extended version upto 64 bits

Instruction size for Cortex – M0 is mostly 16 bits

As far as code density is concern Cortex – M series occupies less amount of code memory let us understand the same by taking example of 16-bit multiplication in 8-bit processor, 16-bit processor and Cortex – M series.

<table>
<thead>
<tr>
<th>MCU/ Processor</th>
<th>No. of instructions required</th>
<th>No. of bytes required for code</th>
<th>Time required in clock cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit</td>
<td>29</td>
<td>48</td>
<td>48</td>
</tr>
<tr>
<td>16-bit</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Cortex – M0</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5.2 Code Density Comparison For 16 Bit Multiplication

Table 5.2 shows the code density comparison[22] for 16-bit multiplication example in different MCUs, detail coding shown in appendix. Clearly one can say that Cortex M series provides better code density.

- Data processing capabilities of Cortex – M series better than that of 8/16 bit MCUs.
  - When it comes to process a data of more than 8-bit, 8-bit MCUs consumes more time to process the same, because they have 8-bit registers, ALU and memories. Stack requirement is high.
  - Same way for data more than 16-bit, 16-bit processor consumes more time to process it, because they have 16-bit registers, ALU and memories. More stack requirement
  - Cortex – M0 has 32-bit registers and memories therefore it process the data upto 32 bit mostly in one clock cycle.
- Addressing modes and memory structure of Cortex – M series much powerful than that of 8/16 bit MCUs.