Chapter 2

Motivation and Objectives

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2.1 Motivation:

As ARM architecture offers following RISC features

- Relatively large register set
- Reduced number of instruction classes
- Simple load – store architecture
- Pipeline architecture

Above features are not commonly available to any conventional microcontroller – that has given the primary motivation to select the ARM core architecture for enhancement and utilizing the performance of it.

A processor core which is capable of dealing with different modes[2][3] of operation like system & user along with privileged modes (FIQ, IRQ, Abort, Undefined, and Supervisor). Privileged modes can be only access by the exception, thereby providing utmost security to different levels.

Power consumption is always been a critical issue when we talk about portable devices, usually in a system whichever devices are available consumes power even though they are not used – that creates unnecessary loss of power. To avoid the loss of power if we can have mechanism whereby we make the devices ON/OFF as per the usage of the system then we certainly save the power to great extent. Mixed (analog & digital) signal processing is now possible with the advent of Programmable System on Chip (PSoC), PSoC are developed by Cypress semiconductors, so one can enjoy the luxury of ARM core with PSoC5[27]. PSoC5 Provides great flexibility of handling analog and digital signals with ARM cortex –M3 core.

Porting the Operating System[35] on ARM core with open source Linux is another motivation by which one can have their own portable Linux based complex embedded machine. After porting the desired OS one can easily enhance the architecture of the ARM and can effectively use the entire system as PC.


2.2 Primary Objectives Of The Research:

Following are the list of major objectives of my research work.

- To differentiate the different ARM architecture and its enhancement.
- To identify the parameters for the improvement in the architecture.
- To look at the power consumption issue in embedded system design.
- To develop effective Branch prediction mechanism for better throughput for multistage pipeline architecture in ARM core.
- To increase the parallelism in ARM7TDMI architecture by embedding the RTOS on it and realizing multitasking functionality, thereby increasing throughput.
- To realize & enhance ARM core for mixed signal processing using Cypress PSoC5 having ARM cortex M core inside it, thereby to design power efficient system with selectable Digital and Analog blocks.
- To develop a real time monitoring & data logging system with different ARM core.
- To enhance the ARM architecture based core by porting Operating System, so that it can work as Linux based complex embedded computing machine having all the features of desktop computing along with varieties of interface for custom design applications.

2.3 ARM Cores Which Are Taken For Consideration Of The Research:

- ARM7/ARM7TDMI
- ARM11
- ARM CORTEX – M Series

2.4 Hardware Used:

- LPC 2138 Evaluation board – NXP
- PSoC 5 Development Kit [CY8CKIT001 – PSoC CY8C55 (PSoC5) family processor module] – Cypress
- RaspberryPi – Model B [Broadcom BCM2835 system on a chip (SoC), which includes an ARM1176JZF-S]
- Arduino UNO – open source electronics prototyping platform
2.5 Tools And Software Used:

- Simplescalar toolset
- KEIL Software
- Flash Magic Software
- PSoC Creator IDE
- Open source operating systems
- Raspbian OS for RaspberryPi and Debian.
- Arduino UNO IDE & Python programming