Chapter- 7

CONCLUSION AND SCOPE OF FURTHER WORK

7.1 Introduction

Minimization of Boolean functions has been an active area of investigations for decades. A good amount of work [3-83] has already been carried out by researchers to develop various paper-and-pencil methods and recently to develop CAD algorithms [92-104] pertaining to Boolean function minimization required in VLSI design. The technology for manufacturing digital circuits has also evolved substantially resulting in need of developing suitable methods of technology dependent minimization methods. The present work is an endeavour to develop a method which is immediately suitable as a pedagogic tool capable of providing a paper-and-pencil solution [118-125] for better insight to the students alongwith its capability to be implemented on multiprocessor system [126-130] so as to reduce the time required for formation of prime implicants during the minimization of a large Boolean function. The work carried out to develop such a method has been presented in the chapters 3 to 6 with the following conclusion.

7.2 Conclusion

Development of the suggested paper-and-pencil method, proposed parallel algorithms alongwith the results obtained by simulation are as under.

1. A novel method of Boolean function minimization has been developed suggesting a new minterm numbering scheme based on the properties of
Binary Reflected Gray Code [119]. It has been shown that the present method can provide a flexible style of writing minterms in a single line or a number of lines and a set of rules to identify adjacent minterms and to form groups leading to minimization of the given Boolean function have also been developed. The better graphical representation has been shown to be useful to select the minimum set of prime implicants (PIs) required to cover the minterms present in the given Boolean function.

II. The proposed method is much generalized so that Karnaugh map can be considered as its special case [121]. Moreover, the proposed method has been shown to be able to provide a planer (2-D) graphical representation of minterms and their adjacencies which is very difficult in K-map method for six or more number of variables [121]. The rules to identify all possible prime implicants and obtaining minimum cover for both completely and incompletely specified Boolean functions have been developed and implemented on various examples. A seven variable example has been solved using the proposed method giving a planer graphical representation of adjacencies which is not possible in case of K-map.

III. The proposed method has been used to implement digital circuits in terms of Ex-OR and Ex-NOR gates if it is not possible to have a AND –OR minimization or owing to design requirements [120] of the given Boolean function. It has been shown that minterms or groups of minterms differing in two bits can be visually identified readily due to flexible and versatile graphical representation of minterms and their adjacencies in the proposed method. The rules to find such two bit differing minterms or groups of minterm and their simplification have been developed from scratch. The
simplification procedure has been implemented on a few numerical examples.

IV. The Variable Entered graphing (VEG) technique [124, 125] has been developed in which a Boolean function of many variables having a few sparsely occurring minterms has been treated as a Boolean function with sufficiently small number of variables resulting in faster and easier minimization by paper-and-pencil. The rules for such conversion of larger Boolean function into smaller one and those of minimization have been developed and implemented on an example.

V. The proposed paper-and-pencil method has been applied to realize Boolean functions using multiplexers and then to a real life problem for minimizing number of keys to be passed to a client in secure internet multicast [123] so that the valid client (in a pay per view service, video-on-demand site, etc.) is able to keep logging on the server while the clients opting out (or terminated due to expiry of term, etc.) can not use the services.

VI. The proposed method has been shown to be better than the K-map method as it provides more flexible graphical representation of minterms and their adjacencies in a planer form [122]. It is also shown [122] that the proposed paper-and-pencil method is better than QM Method if the minimization is being carried out on paper as the proposed method being graphical gives the minimized expression by mere inspection without drawing any tables and then solving the covering problem drawing a grid to obtain prime implicants.

VII. The proposed method has been augmented to be implemented in parallel [126, 127]. It has been shown that the SPMD based algorithm which is executed on every node, namely, "recursive_reflection algorithm" generates
all possible implicants of the given function using the reflection property of
the BRGC. It has been simulated on a PIV computer and have shown to
provide excellent time saving [127] in comparison to serial implementation.
A number of Boolean minimization examples have been solved simulating
the multiprocessor working.

VIII. The time saving obtained in [127] has been further improved by carrying out
a simple load balancing technique amongst the nodes of multiprocessor and
better results in terms of time saving and speedup are obtained [128] for the
same examples as those considered in [127]. A dynamic load balancing
technique similar to that of [150] is when used with the proposed parallel
algorithm [129] has yielded still better time saving and speedup than that of
[128].

IX. Another parallel method exploiting the reflection and unit distance
properties of BRGC in a similar fashion to those of [118-129] has been
developed circumventing the use of recursion at every node thus providing
better speedup [130]. The suggested minterm numbering scheme has been
shown to have facilitated development of a general formula to calculate the
adjacent minterms of a given minterm independently for each bit (variable
of the given Boolean function). This scheme results in more saving of
computation time as the pairs in the suggested method are now obtained
analytically (numerically) without forming the matrix as shown in [127-
129].

X. The suggested parallel method [130] has been shown to have linear increase
in parallel run time with number of product terms whereas in the CAD tools
based on QM method [91, 103] the run time varies exponentially. Further,
the parallel run time of the suggested method remains almost constant by varying the number of inputs from 10 to 60 keeping number of product terms fixed. Hence it can be safely inferred that run time of the proposed parallel algorithm is independent of number of variables for a given onset and is a linear function of the number of product terms present in the onset.

The scope of further work in the area of the proposed method can be many a few of which are summarized as under.

7.3 Scope of Further Work

Further investigations can be carried out in the areas related to extension/application of the proposed method to various design steps of upcoming technology of chip design (VLSI design), distributed computing, etc. A few of these are listed below.

I. Minimization of Multi Output Boolean Functions

The proposed paper-and-pencil method and its parallel algorithms suggested and implemented in the present work can be extended to the case of multi output Boolean function minimization for Programmable Logic Arrays (PLA) and Programmable Array Logic (PAL) circuits.

II. Multilevel Logic Synthesis

The modern implementation (chip manufacturing) technologies of digital circuit use multilevel logic synthesis to obtain technology dependent reduction in the described combinational circuit. Most of the CAD tools available for logic synthesis use two-level Boolean function minimization in some phase or other
of synthesis, e.g., the synthesis tool MIS II [152] developed at University of California at Berkeley uses ESPRESSO [91] as a subroutine. The proposed two-level Boolean minimization method can as well be used as a supporting program to other logic synthesis programs, especially to those [106] which carry out logic synthesis on parallel basis. Thus, the proposed parallel algorithm can be extended to design of multilevel circuits.

III. Extension for Simplification in Terms of Ex-OR and/or Ex-NOR Gates

With the advancement in the implementation technology of digital circuits it has now become possible to use simplification of the Boolean function in terms of Ex-OR and/or Ex-NOR forms or in Ex-OR Sum of Product (ESOP) form more beneficially as compared to minimization in AND-OR form for certain cases [77]. The proposed paper-and-pencil method has been shown to be capable of simplifying the given Boolean function in ESOP form [120]. The rules of finding second level adjacencies and subsequent simplification have been well developed [120] which can be further investigated to develop a parallel algorithm for ESOP simplification.

IV. Investigation for Better Load Balancing Techniques

Though two load balancing schemes have been proposed and implemented on PARABOOMIG-I, further investigation can be carried out to formulate a better one giving better performance. The proposed parallel algorithm PARABOOMIG-I [127-129] which executes a recursive algorithm on every node on SPMD basis can be further investigated to reduce the depth of
Recursion so that run time of the algorithm can be reduced further and better load balancing performance can be achieved.

V. Investigation of Other Topologies of Multiprocessor Systems for Better Performance of the Proposed Method

It has been mentioned in section 6.2.2 of the chapter 6 that the best suitable multiprocessor topology for implementation of PRABOOMIG-II would have been a ring but due to high communication cost (round trip delay in a copper ring) the working of ring, as required in the proposed algorithm, has been simulated on a star topology [129]. Extensive research in the area of optical interconnects [153] for TFlop/sec Parallel Supercomputer is in progress. The proposed method can be further investigated for its possible implementation on an optical ring topology where it is possible for a node to send its packet appending it at the end of packet sent by the previous node thus not waiting for complete roundtrip delay.

VI. Application as a Web Based Minimizer

The proposed method can be readily implemented in distributed environment as a web based program to minimize the Boolean functions similar to that of [154]. Due to parallelism offered by the proposed method computational capabilities of two processors, namely, the server hoisting the program and the client requesting for minimization can be exploited to obtain better time saving using the proposed parallel method.
VII. Implementation of the Proposed Algorithm in Distributed Environment to Achieve Cost Reduction

Multiprocessor systems are expensive to procure and maintain, therefore, as a cost reduction measure the proposed parallel algorithms PARABOOMIG -I and PARABOOMIG -II can readily be implemented in distributed environment using Java-Based Framework on similar lines as given in [155] because now-a-days most of the moderately sized institutions have a LAN facility on their campuses.

Lastly, the proposed parallel two-level Boolean function minimization algorithms are equally applicable to all those systems which require a Boolean function minimization phase in their working.