APPENDIX 1

AT89C2051 MICROCONTROLLER

The AT89C2051 is a low-voltage, high performance CMOS 8-bit microcomputer with 2K Bytes of Flash programmable and erasable read only memory. The device is manufactured using ATMEL high-density nonvolatile memory technology and is compatible with the industry standard MCS-51 instruction set. Combining a versatile 8-bit CPU with flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer, which provides a highly flexible and cost effective solution to many embedded control applications.

A1.1 FEATURES

- Compatible with MCS®-51 Products
- 2K Bytes of Reprogrammable Flash Memory – Endurance: 1,000 Write/Erase Cycles
- 2.7V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial UART Channel
• Direct LED Drive Outputs
• On-chip Analog Comparator
• Low-power Idle and Power-down Modes
• Green (Pb/Halide-free) Packaging Option

A1.2 BLOCK DIAGRAM OF MICROCONTROLLER AT89C2051

Figure A1.1 Block diagram of 8 bit microcontroller 89C2051

A1.3 OPERATING DESCRIPTION

The detailed description of the AT89C51 is as given below:

• Memory map and register
• Timer/counter
Memory map and registers

The atm89C51 has separate address paces for program and data memory. The program and data memory can be upto 64KB long. The lower 4k program memory can reside on-chip.

The ATM89C51 has 129 bytes of on-chip RAM plus a number of special function registers. The lower 128 bytes can be accessed either by direct addressing or by indirect addressing.

The lower 128 bytes of RAM can be divided into three segments as

- Register banks 0-3
- Bit addressable area
- Scratch pad area.

A1.4 SPECIAL FUNCTION REGISTERS

Special function registers are located in the upper 128 bytes direct addressing area.

(a) Accumulator (ACC)

ACC is the accumulator that registers the mnemonics for accumulator specific instructions ; however, refer to the accumulator simply as A.
(b) **Register B**

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

(c) **Stack Pointer (SP)**

The stack pointer register is eight bit wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in the on-chip RAM, the stack pointer is initialized to 07H after a reset; this causes the stack to being at location 08H.

(d) **Flash Programming**

There are three methods of erasing or programming of the FLASH memory that may be used. First, the FLASH may be programmed or erased in the end-user application by calling low level routine through a common entry point in the Boot ROM.