Chapter 7

Digital Signal Processor based Hardware Implementation of Current Error Space Phasor based Hysteresis Controller for Two-level Shunt Active Power Filter

A laboratory scale prototype model of the proposed controller based SAPF has been developed using DSP TMS320LF2407A. IGBT based two-level converter is fabricated and used as SAPF. Three-phase diode bridge rectifier with capacitor filter and resistive load is used as non-linear load (harmonic current generating load). Reference compensating currents are generated by Fryze current computation technique using DSP. As the proposed current controller based SAPF is versatile in nature, it can work for any reference compensating current generation schemes as depicted from results of Chapter-5 and Chapter-6. The current error space phasor based hysteresis controller for two-level SAPF is experimentally implemented for sector change detection without using outer hysteresis band as well as with outer hysteresis band. The proposed controller based SAPF, without using outer hysteresis band is experimentally implemented with sector change detection by instantaneous values of three-phase voltages at the point of common coupling. The another logic (discussed in Chapter-4) for identifying necessary sector changeovers (without using outer hysteresis band), sector change detection by instantaneous values of voltages at the point of common coupling, is not implemented practically as it suffers drawbacks of not being able to detect the frequency change between two consecutive zero crossing detections, which is quite possible in practical conditions. Reference compensating current calculation scheme along with proposed current controller logic is implemented in DSP. Entire
code for successful implementation of proposed SAPF is developed in assembly language using code composer studio. General purpose input/output (GPIO) port B of DSP is used for providing gates signals.

Figure 7.1 shows the block diagram for experimental implementation of proposed controller based two-level SAPF. Three LEM Hall-effect voltage transducers are used for sensing the three-phase voltages at the point of common coupling. Similarly, three LEM Hall-effect current transducers are used to sense the non-linear load currents and three current transducers are used to sense the actual compensating currents (SAPF currents). As DSP has unipolar analog to digital converter (ADC), op-amp based external offset circuit is used to make the sensor outputs compatible with ADC of the DSP. Depending on the current error between actual compensating current and reference compensating current the controller logic generates appropriate control signals based on voltage vectors to be switched. These control signals for control of SAPF are made available at the GPIO pins of DSP. These control signals are then provided to gate driver circuit (with optical isolation) which ensures proper and adequate gate signals for switching of the IGBT based converter of SAPF. Gate driver circuit also generates the desired dead-band of approximately 2 $\mu$s between the gate signals of the IGBTs of the same leg of the converter. This ensures the complementary nature of switching the top and bottom IGBT of the same leg of the converter and avoids the short circuit in the converter. The dc-link of SAPF is supplied from the PCC, and it remains stable during the operation of SAPF. Hence, separate dc-link capacitor voltage control circuitry and control algorithm is not required. However, the same is recommended in practice for better performance of SAPF as discussed in Chapter-3. Experimental results are presented for steady state and dynamic conditions of SAPF. It is established from the experimental results that the proposed controller based SAPF operates satisfactorily and compensates for the current harmonics present in the system.

### 7.1 Hardware implementation

The experimental set-up is shown in figures 7.2 and 7.3. The laboratory scale prototype is developed for three-phase, three-wire system. Supply is given to the set-up through a three-phase variac for operation at lower voltage. Various components of the set-up are explained below.
Figure 7.1: Block diagram for experimental set-up of current error space phasor based hysteresis controller for two-level shunt active power filter

Figure 7.2: View-1 of experimental set-up of current error space phasor based hysteresis controller for two-level shunt active power filter
7.1.1 Sensor board

Sensing of signals is an important aspect for appropriate operation of the system. The current and voltage signals are sensed using LEM Hall-effect current and voltage transducers, respectively. Total of nine signals \( (E_a, E_b, E_c, i_{la}, i_{lb}, i_{lc}, i_{ca}, i_{cb} \text{ and } i_{cc}) \) are sensed continuously. Thus six LEM current transducers and three LEM voltage transducers are used for signal sensing. In order to have proper orientation of the hardware set-up, two separate sensor boards are developed. A sensor board is used for sensing PCC voltages \( (E_a, E_b, E_c) \) and load currents \( (i_{la}, i_{lb}, i_{lc}) \) of each phase respectively, while another sensor board is used for sensing SAPF compensating currents \( (i_{ca}, i_{cb} \text{ and } i_{cc}) \). A sensor board consists of sensors [149],[150] and power supply for sensors. As an example, connections of a voltage and a current sensor with power supply is shown in figure 7.4. In similar manner connections are made for each of the voltage and current sensors used in the system.
7.1.2 Offset circuit

The DSP TMS320LF2407A is a unipolar DSP working in the range of 0-3.3 V. As the output of the sensors is ac signal, negative half cycle of the signals will get clamped if given directly to the ADC of DSP as shown in figures 7.5. Thus there will be loss of information and the system will not work properly. Therefore the sensed signals are given an offset to make them unipolar. Proper sensing of signals is done by the ADC after providing offset as shown in 7.6. These figures show waveforms taken out from DAC of DSP. In this case the value of dc offset is 1.65 volts provided by the offset circuit. Offset circuit is realized using IC LM-741. Figure 7.7 shows the connections of single integrated circuit (IC) LM-741 operational amplifier used for providing offset to single signal. Similarly connections are made for nine LM-741 ICs, as there are nine signals sensed as mentioned above. Also, the sensors are calibrated taking into consideration that during experimentation the maximum possible amplitude of input to DSP which is output of sensor along with dc offset of 1.65 V does not exceed 3.3 V during the course of experimentation in order to protect the DSP.
Figure 7.5: (a) PCC voltages without offset ($E_a$; first trace, $E_c$; second trace) [Y-axis: 40 V/div.(first and second trace), X-axis: 10 ms/div.] (b) Non-linear load currents without offset ($i_{la}$; first trace, $i_{lc}$; second trace) [Y-axis: 2 A/div.(first and second trace), X-axis: 10 ms/div.]

Figure 7.6: (a) PCC voltages with offset ($E_a$; first trace, $E_c$; second trace) [Y-axis: 40 V/div.(first and second trace), X-axis: 10 ms/div.] (b) Non-linear load currents with offset ($i_{ta}$; first trace, $i_{tb}$; second trace) [Y-axis: 2 A/div.(first and second trace), X-axis: 10 ms/div.]
7.1.3 Digital signal processor TMS320LF2407A based implementation of reference compensating current generation method and proposed controller

TMS320LF2407A is a fixed-point DSP. This DSP is used to implement reference compensating current generation method and the current error space phasor based hysteresis controller with the help of assembly language coding. Assembly language code is developed using code composer studio (CCS). Signals from offset circuit are provided to the 10-bit analog to digital converter (ADC) of DSP. All the nine signals as mentioned above, which are input to the ADC are converted in to digital form and used for further processing by DSP. For effective implementation of the DSP code in assembly language, all the signals and data are to be processed uniformly. Hence, 4.12 format of data processing is used for the assembly language code [138], because all the SAPF control quantities are not more than four times their nominal value. All mathematical computations in DSP are done using accumulator of DSP which is 32-bit and divided into higher and lower accumulator each of 16-bit. Figure 7.8 shows the content of accumulator (either higher or lower accumulator) in 4.12 format, where 4 bit represent integer part, while 12 bits are the fractional part of the data to be processed. As 12-bits are occupied for the fractional part of the data, preciseness in handling of data is achieved. Any parameter inside the DSP is viewed with the help of 12-bit digital to analog converter (DAC). Fryze current computation technique is
used for generating reference compensating currents and the logic used for implementing this method using DSP is mentioned in the flow chart shown in figure 7.9. The generated reference compensating currents are then compared with the actual compensating currents, which are provided to the DSP in order to generate current error. These current errors in identical phases are then combined to generate current error space phasor. Depending on this current error space phasor, the proposed current controller logic generates gate signals (in the form of pulses at the GPIO pins of the DSP) for switching of the SAPF, such as to ensure that actual compensating current tracks the reference compensating current and hence the current error space phasor is restricted within desired hexagonal boundary. Output of the GPIO pins are provided to the gate driver cards which ensures appropriate firing of the SAPF.

Figure 7.9: Flow chart of Fryze current computation technique
7.1.4 Gate driver board and two-level converter of SAPF

Gate driver board consists of gate driver card for each leg of the SAPF. Each gate driver card consists of gate driver circuitry along with power supply, as shown in figure 7.10. Gate driver card provides a dead band of 2 $\mu$S and over current protection ($V_{CE(SAT)}$ protection) to IGBT. Each gate driver card is used for switching of a IGBT module (two IGBTs) of one leg of SAPF. Thus three gate driver cards are used for switching of SAPF. The entire gate driver card board consists of four gate driver cards, where one card is kept extra. Two-level converter of SAPF is realized using three dual-pack IGBT modules SKM75GB12T4 as shown in figure 7.11. These modules are mounted on heat sink to ensure appropriate heat dissipation. Each phase output of the converter is connected to respective phase of PCC through SAPF inductors shown in figure 7.1.
7.2 Experimental results

The experimentation is carried out on the laboratory prototype scale at supply voltage 30 V with fundamental frequency 50 Hz. The non-linear load comprises of three-phase diode bridge rectifier with filter capacitance 1000 $\mu$F and resistive load of 100 $\Omega$ (variable). Load side inductance ($L_{load}$) is 0.66 mH, while source side inductance is 50 $\mu$H (Figure 7.1). As per the design considerations of SAPF explained in Chapter 3 of the thesis, value of SAPF inductor ($L_{filter}$) for practical implementation is taken as 2.11 mH and the dc-link capacitor ($C_{dc}$) is taken as 3300 $\mu$F.

7.2.1 PCC voltage and load current

Figures 7.12 and 7.13 show the PCC voltage and load currents of the system. Results ensure that phase shift and phase sequence is proper.

Figure 7.12: Results for phase A: PCC voltage ($E_a$; first trace) and load current ($i_{la}$; second trace) [Y-axis: 10 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]

Figure 7.13: PCC voltage ($E_a$; first trace) and load currents for all phases ($i_{la}$; second trace, $i_{lb}$; third trace, $i_{lc}$; fourth trace) [Y-axis: 50 V/div.(first trace), 5 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]
7.2.2 Sensing of various parameters and processing in DSP

It is very much important that the system parameters which are provided to the DSP through sensors and offset circuit are in line with the actual ones. Figure 7.14 shows the PCC voltage measured by differential voltage probe and as viewed at the DAC of DSP, while figure 7.15 shows the load current as measured by current probe and as viewed at the DAC. Results clearly indicate the effectiveness of the data acquisition system (sensors and offset circuit) and data processing system as the actual parameters are in line with the parameters fed to the DSP and hence there is no data loss.

Figure 7.14: PCC voltage $E_a$: (measured by probe; first trace) and (DAC output; second trace) [Y-axis: 10 V/div.(first trace), 0.5 V/div.(second trace), X-axis: 0.005 s/div.]

Figure 7.15: Load current $i_{la}$: (measured by probe; first trace) and (DAC output; second trace) [Y-axis: 1 A/div.(first and second trace), X-axis: 0.005 s/div.]
7.2.3 Reference compensating currents

The reference compensating currents are generated by Fryze current computation technique. By the compensation principle of SAPF, if reference compensating current is subtracted from load current, source current is achieved (which is supposed to be sinusoidal in shape). As shown in figure 7.16 load current ($i_{la}$) and reference compensating current ($i^*_{ca}$), both signals output from DAC of DSP, are subtracted by math function of digital storage oscilloscope, which gives source current ($i_{sa}$) and is as desired. Hence this proves the correctness of the reference compensating current generated. Similar results are obtained for all the phases. Reference compensating currents for all the phases ($i^*_{ca}$, $i^*_{cb}$ and $i^*_{cc}$) are shown simultaneously in figure 7.17.

![Figure 7.16: Load current ($i_{la}$; first trace), Source current ($i_{sa}$; second trace) and Reference compensating current ($i^*_{ca}$; third trace) [Y-axis: 1 A/div.(first, second and third trace), X-axis: 0.005 s/div.]](image)

![Figure 7.17: PCC voltage ($E_a$; first trace) and Reference compensating currents of all phases ($i^*_{ca}$; second trace, $i^*_{cb}$ third trace, $i^*_{cc}$; fourth trace) [Y-axis: 50 V/div.(first trace), 1.2 A/div.(second, third and fourth trace), X-axis: 0.01 s/div.]](image)
### 7.2.4 Behavior of the system without compensation

Figure 7.18 shows behavior of the system when SAPF is not connected. It is clearly visible from the results that non-linear load has distorted the source current. As seen from the results without compensation the source current $i_{sa}$ is similar to non-linear load current $i_{la}$. These results indicate need of the SAPF to compensate for the harmonics introduced in the system due to non-linear load. The same non-linearity is observed in the source current for other phases (i.e. B and C) as well. Normalised harmonic spectrum of $i_{la}$ for one cycle is shown in figure 7.19 and it has THD of 40.17%. Dominating harmonics of the order $6n \pm 1$ (n= 1,2,3,...) are quite evident from figure 7.19 as the load is a six-pulse rectifier.

![Figure 7.18: System behavior without compensation: PCC voltage ($E_a$; first trace), Source current ($i_{ca}$; second trace), Load current ($i_{la}$; third trace) and Reference compensating current ($i_{ca}^*$; fourth trace) [Y-axis: 20 V/div.(first trace), 2 A/div.(second trace), 2.5 A/div.(third trace), 1.25 A/div.(fourth trace), X-axis: 0.005 s/div.]

![Figure 7.19: Normalised harmonic spectrum of $i_{la}$ [Y-axis: normalised amplitude 0.2/div., X-axis: order of harmonics]]
7.2.5 Performance of current error space phasor based hysteresis controller (without using outer hysteresis band for sector change detection) for two-level SAPF

Experimental verification of the performance of current error space phasor based hysteresis controller for two-level SAPF with sector change detection without using outer hysteresis band is presented here. Sector change detection logic by instantaneous values of three-phase voltages at the point of common coupling is used for satisfactory operation of the proposed controller based SAPF. Figure 7.20, shows the necessary sector changes detected by this logic (where \( E_a, E_b, E_c \) and sector are viewed from DAC of DSP). This performance is quite matching with figure 4.22 discussed in chapter-4 for sector change detection logic. The sector change is taking place as intended. Slight unbalance in three-phase supply voltages at the PCC is observed which is a practically quite possible situation. Figures 7.21 and 7.22 show the behavior of proposed controller (without using outer hysteresis band) based two-level SAPF. It is verified from the results that the SAPF compensates for the harmonics present in the load current and thereby ensuring sinusoidal source current. The proposed controller based SAPF reduces the THD in source current from 40.17 % to 7.13 %. There is no phase shift between PCC voltage (\( E_a \)) and source current (\( i_{sa} \)) after compensation, which is shown by figure 7.23. The proposed controller based SAPF provides satisfactory compensation for all the phases, which is evident from figures 7.24 and 7.25. Figure 7.26 shows SAPF output voltage (\( V_{ab} \)) along with actual compensating current (\( i_{ca} \)), it is evident that there is no random switching and dc-link voltage of SAPF remains stable (as \( V_{ab} \) is stable). The proposed controller based SAPF ensures that actual compensating current track the reference compensating current which is evident from figure 7.27. The current error space phasor is shown in figure 7.28. It is quite evident that current error space phasor remains inside the hexagonal boundary. The normalised harmonic spectrum (FFT) of source current is shown in figure 7.29. Where it is seen that all the dominating harmonics (as seen in figure 7.19) are eliminated by the SAPF.
Figure 7.20: PCC voltages for all phases ($E_a$, $E_b$ and $E_c$; first trace) and Sectors of voltage space phasor structure for two-level SAPF (sectors; second trace) [Y-axis: 0.5 V/div.(first trace), sectors (second trace), X-axis: 0.005 s/div.]

Figure 7.21: Performance of proposed controller (without using outer hysteresis band) based two-level SAPF: PCC voltage ($E_a$; first trace), Source current ($i_{sa}$; second trace), Load current ($i_{la}$; third trace) and Actual compensating current ($i_{ca}$; fourth trace) [Y-axis: 50 V/div.(first trace), 5 A/div.(second trace), 2 A/div.(third trace), 5 A/div.(fourth trace), X-axis: 0.005 s/div.]
Figure 7.22: Performance of proposed controller (without using outer hysteresis band) based two-level SAPF: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca^*}$; fourth trace) [Y-axis: 5 A/div.(first trace), 5 A/div.(second trace), 2 A/div.(third trace), 1 A/div.(fourth trace), X-axis: 0.005 s/div.]

Figure 7.23: PCC voltage ($E_a$; first trace) and Source current ($i_{sa}$; second trace) [Y-axis: 5 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]
Figure 7.24: Source current ($i_{sa}$; first trace) and Actual compensating currents of all phases ($i_{ca}$; second trace, $i_{cb}$ third trace, $i_{cc}$; fourth trace) [Y-axis: 5 A/div.(first trace), 2.5 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]

Figure 7.25: PCC voltage ($E_a$; first trace) and Source currents of all phases ($i_{sa}$, $i_{sb}$, $i_{sc}$; second trace) [Y-axis: 20 V/div.(first trace), 3 A/div.(second trace), X-axis: 0.005 s/div.]
Figure 7.26: SAPF output voltage ($V_{ab}$; first trace) and Actual compensating current ($i_{ca}$; second trace) [Y-axis: 20 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]

Figure 7.27: Overlapped waveform for $i_{ca}$ and $i_{ca}^*$ [Y-axis: 1 A/div., X-axis: 0.005 s/div.]

Figure 7.28: Current error space phasor [Y-axis: 0.25 A/div., X-axis: 0.25 A/div.]
7.2.6 Effects of hysteresis band variation on the performance of proposed controller (without using outer hysteresis band for sector change detection) based two-level SAPF

Performance of the proposed controller based SAPF is studied for variation in hysteresis band. Figures 7.30, and 7.31 show the behavior of SAPF for different hysteresis bands. It is clearly depicted from the results that as hysteresis band is increased the switching frequency reduces which is in line with the nature of proposed controller given by (4.8). The source current is seen more smoother for smaller band and the switching is found more. In practice also there is always a trade-off between smoothness of current and switching losses of the SAPF, while choosing the particular band for current controller.

Figure 7.30: Effect of variation in hysteresis band: SAPF output voltage ($V_{ab}$; first trace), Source current ($i_{sa}$; second trace), Load current ($i_{lb}$; third trace) and Actual compensating current ($i_{ca}$; fourth trace) [Y-axis: 50 V/div.(first trace), 5 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]
7.2.7 Transient behavior of proposed controller (without using outer hysteresis band for sector change detection) based SAPF under load variations

Performance of proposed controller based SAPF is studied for changes in load. The load on the rectifier is suddenly changed in order to create transient conditions. Figure 7.32 shows the behavior of SAPF for decrease in load (by suddenly increasing the load resistance). Effect of decrease in load is clearly visible from the results (as shown in 7.32). It is evident from the results that SAPF compensates satisfactorily when load is suddenly changed. Performance of SAPF for increase in load is depicted from Figure 7.33. During transient conditions caused by sudden load change, the SAPF does not lose control and actual compensating current tracks the reference compensating current. Hence the compensation provided by the SAPF does not suffer during transient conditions. Thus, it is evident from the results of figures 7.32 and 7.33 that proposed controller based SAPF operates satisfactorily and provides compensation to the source current as desired, under transient conditions also.
Figure 7.32: Transient behavior of proposed controller (without using outer hysteresis band) based SAPF for decrease in load: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca^*}$; fourth trace) [Y-axis: 5 A/div.(first trace), 2 A/div.(second, third and fourth trace), X-axis: 0.01 s/div.]

Figure 7.33: Transient behavior of proposed controller (without using outer hysteresis band) based SAPF for increase in load: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca^*}$; fourth trace) [Y-axis: 5 A/div.(first trace), 2 A/div.(second, third and fourth trace), X-axis: 0.01 s/div.]
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7.2.8 Performance of current error space phasor based hysteresis controller (Using outer hysteresis band for sector change detection) for two-level SAPF

Experimental results of the performance of current error space phasor based hysteresis controller for two-level SAPF with sector change detection using outer hysteresis band are shown here. Effectiveness of the sector change detection logic using outer hysteresis band is depicted from the sector changeovers shown in figure 7.34. It is also to be noted that the sector change detection shown in figure 7.20 is possible to detect even when SAPF is not turned on, whereas the sector change detection shown in figure 7.34 is only possible to detect once SAPF is turned on, because the sector change is detected based on the movement of current error space phasor. The sector change is detected here from the current space phasor only and with the outer hysteresis band. No information on three-phase voltages is required in this case to detect the sector change. Unbalance in three-phase voltages is quite evident in the practical situation from figure 7.34. In the proposed controller based SAPF, the current error is allowed to move out of the hexagonal boundary in order to hit the outer band, for detection of necessary sector changeovers. This affects slightly on compensation provided by SAPF. Hence, it is observed from the that smoothness in current waveform shown in figure 7.34, is less as compared to that presented in figure 7.21. Behavior of proposed controller based two-level SAPF is shown in figures 7.35 and 7.36. It is evident from the results that the SAPF compensates for the harmonics present in the load current and thereby ensuring sinusoidal source current. Figure 7.37 indicates that there is no phase shift between PCC voltage ($E_a$) and source current ($i_{sa}$) after compensation. Performance of the proposed controller based SAPF for all the phases is shown in figures 7.38. SAPF output voltage ($V_{ab}$) along with actual compensating current ($i_{ca}$) is shown in figure 7.39. It is evident from the results that there is no random switching and dc-link voltage of SAPF remains stable (as $V_{ab}$ is stable). It is depicted from the figure 7.40, the proposed controller based SAPF ensure that actual compensating current tracks the reference compensating current. The current error space phasor is shown in figure 7.41. The movement of current error outside the hexagonal boundary is visible more in figure 7.41 as compared to that shown in figure 7.28. This is due to the nature of proposed controller based SAPF, which allows the movement of current error space phasor outside the hexagonal boundary for detecting necessary sector changeovers. The normalised harmonic spectrum (FFT) of source current is shown in figure 7.42. The proposed controller based SAPF reduces the THD in source current from 40.17 % to 7.45 %.
Figure 7.34: PCC voltages for all phases ($E_a$, $E_b$ and $E_c$; first trace) and Sectors of voltage space phasor structure for two-level SAPF (sectors; second trace) [Y-axis: 10 V/div.(first trace), sectors (second trace), X-axis: 0.005 s/div.]

Figure 7.35: Performance of proposed controller (Using outer hysteresis band) based two-level SAPF : PCC voltage ($E_a$; first trace), Source current ($i_{sa}$; second trace), Load current ($i_{la}$; third trace) and Actual compensating current ($i_{ca}$; fourth trace) [Y-axis: 10 V/div.(first trace), 2 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]
Figure 7.36: Performance of proposed controller (Using outer hysteresis band) based two-level SAPF: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca*}$; fourth trace) [Y-axis: 2 A/div.(first trace), 2 A/div.(second trace), 1 A/div.(third trace), 1 A/div.(fourth trace), X-axis: 0.005 s/div.]

Figure 7.37: PCC voltage ($E_a$; first trace) and Source current ($i_{sa}$; second trace) [Y-axis: 5 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]
Figure 7.38: PCC voltage ($E_a$; first trace) and Source currents of all phases ($i_{sa}$; second trace, $i_{sb}$; third trace, $i_{sc}$; fourth trace) [Y-axis: 10 V/div.(first trace), 2 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]

Figure 7.39: SAPF output voltage ($V_{ab}$; first trace) and Actual compensating current ($i_{ca}$; second trace) [Y-axis: 20 V/div.(first trace), 1 A/div.(second trace), X-axis: 0.005 s/div.]
Figure 7.40: Overlapped waveform for $i_{ca}$ and $i_{ca}^*$ [Y-axis: 0.5 A/div., X-axis: 0.005 s/div.]

Figure 7.41: Current error [Y-axis: 0.15 A/div., X-axis: 0.15 A/div.]

Figure 7.42: Normalised harmonic spectrum of $i_{sa}$ [Y-axis: normalised amplitude 0.2s/div., X-axis: order of harmonics]
7.2.9 Effects of hysteresis band variation on the performance of proposed controller (Using outer hysteresis band for sector change detection) based two-level SAPF

Behavior of the proposed controller based SAPF is studied for variation in both, outer hysteresis as well as inner hysteresis band. Performance of the proposed controller based SAPF for different hysteresis bands is depicted from figures 7.43, 7.44, 7.45, and 7.46. Inner hysteresis band and outer hysteresis band for A-phase is shown with results to analyze change in hysteresis band. Results indicate that increase in hysteresis bands decreases the switching frequency and on the other hand it reduces the smoothness of the compensated current, which is the inherent nature of proposed controller as given by (4.8). In practice there is always a trade-off between quality of current waveform and switching losses while deciding the hysteresis band. Figures 7.43, 7.44, 7.45 and 7.46 are the results shown for gradual increment in the hysteresis bands of the proposed controller.

Figure 7.43: Effect of variation in hysteresis band: SAPF output voltage ($V_{ab}$; first trace), Source current ($i_{sa}$; second trace), [Y-axis: 20 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]
Figure 7.44: Effect of variation in hysteresis band: SAPF output voltage ($V_{ab}$; first trace), Source current ($i_{sa}$; second trace). [Y-axis: 20 V/div.(first trace), 2 A/div.(second trace), X-axis: 0.005 s/div.]

Figure 7.45: Effect of variation in hysteresis band: PCC voltage ($E_a$; first trace) and Source currents of all phases ($i_{sa}$; second trace, $i_{sb}$; third trace, $i_{sc}$; fourth trace) [Y-axis: 20 V/div.(first trace), 3 A/div.(second, third and fourth trace), X-axis: 0.005 s/div.]
Figure 7.46: Effect of variation in hysteresis band: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca}^*$; fourth trace) [Y-axis: 2 A/div.(first trace), 2 A/div.(second trace), 1 A/div.(third trace), 1 A/div.(fourth trace), X-axis: 0.005 s/div.]

7.2.10 Transient behavior of proposed controller (Using outer hysteresis band for sector change detection) based SAPF under load variations

Performance of proposed controller based SAPF is studied for changes in load. Transient conditions are achieved by suddenly changing the load on the rectifier. It is evident from figure 7.47 that SAPF does not loose control and actual compensating current tracks the reference compensating current during transient conditions. Figures 7.48 and 7.49 shows the behavior of SAPF for decrease in load. Effect of decrease in load (by increasing the load resistance) clearly visible from the results (as shown in 7.48 and 7.49). Performance of SAPF for increase in load (by decreasing the load resistance) is depicted from figure 7.50 and 7.51. Thus, it is depicted from the results that compensation provided to the source current by proposed controller is satisfactory, under transient conditions also.
Figure 7.47: Overlapped waveform for $i_{ca}$ and $i_{ca}^*$ during transient conditions [Y-axis: 1 A/div., X-axis: 0.02 s/div.]

Figure 7.48: Transient behavior of proposed controller based SAPF for decrease in load: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca}^*$; fourth trace) [Y-axis: 2 A/div. (first, second, third and fourth trace), X-axis: 0.02 s/div.]
Figure 7.49: Transient behavior of proposed controller based SAPF for decrease in load: SAPF output voltage ($V_{ab}$; first trace), Source current ($i_{sa}$; second trace), Load current ($i_{la}$; third trace) [Y-axis: 50 V/div.(first trace), 2 A/div.(second and third trace), X-axis: 0.01 s/div.]

Figure 7.50: Transient behavior of proposed controller based SAPF for increase in load: Source current ($i_{sa}$; first trace), Load current ($i_{la}$; second trace), Actual compensating current ($i_{ca}$; third trace) and Reference compensating current ($i_{ca^*}$; fourth trace) [Y-axis: 2 A/div.(first, second, third and fourth trace), X-axis: 0.02 s/div.]
Figure 7.51: Transient behavior of proposed controller based SAPF for increase in load: SAPF output voltage ($V_{ab}$; first trace), Source current ($i_{sa}$; second trace), Load current ($i_{la}$; third trace) [Y-axis: 50 V/div. (first trace), 2 A/div. (second and third trace), X-axis: 0.01 s/div.]

Comparative performance of current error space phasor based hysteresis controller SAPF for harmonic currents in the source current is given in table 7.1

Table 7.1: Experimental performance of current error space phasor based hysteresis controller for two-level SAPF

<table>
<thead>
<tr>
<th>% THD of $i_{sa}$ without SAPF</th>
<th>% THD of $i_{sa}$ with SAPF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Using outer hysteresis band</td>
<td>Using outer hysteresis band</td>
</tr>
<tr>
<td>40.17</td>
<td>7.13</td>
</tr>
</tbody>
</table>

The actual values of THD can further be improved (reduced) by proper professional wiring and compact fabrication of the circuit, avoiding mismatch in dead bands, noise reduction, by further reducing the hysteresis band and use of faster DSP, etc. The % THD of $i_{sa}$ seems to be slightly more in case of sector change detection by outer hysteresis band, this is because in a fundamental cycle current error goes out side the inner hexagonal band six times, for detecting sector change, this has effect on the shape of the source current (compensated current). However, the later technique (detecting sector change by outer hysteresis band will put a foundation for extension of proposed controller application in multi-level converter based SAPF, as there it was not possible to detect sector change from values of three-phase voltages.

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