CHAPTER 7

CONCLUSION

7.1 INTRODUCTION

The silicon based microelectronics industry has been growing rapidly for the past four decades with the continual shrinking of transistor dimensions following the Moore’s law. Unfortunately, fundamental physical limits have heralded the end of the conventional linear scaling of transistor dimensions, and a new era of MOSFET scaling constrained by power dissipation and process-induced variations is the current trend already available. Dual Material Surrounding gate MOSFETs is believed to be the ultimate field effect transistor that is scalable to the nanometer regime. Analysis and simulation of the proposed Dual Material Surrounding gate MOSFETs has been carried out and their performance are compared with single Material Surrounding gate MOSFETs. The compact model for the Short Channel Effects (SCEs) for DMSG MOSFETs has been introduced.

7.2 SALIENT FEATURES OF THE THESIS

- Surface Potential Model

Analytical model of surface potential along the channel in a FD DMSG MOS device is modeled by solving the 2-D Poisson’s equation using a parabolic approximation. The model predicts the creation of a step in the channel potential profile due to the co-existence of two different materials having a finite work function difference and controllable gate lengths. The
existence of mobile carriers is neglected. The shift in the surface channel potential minima position is negligible with increasing drain biases. This leads to excellent immunity against SCE like DIBL and channel length modulation (CLM). It is shown that the electric field in the channel at the drain end is lowered leading to reduced hot-carrier effect. The channel potential profile can be tuned by “gate-material engineering”, i.e., the dependence of surface potential work functions and the lengths of the two gate metals. The model includes the effect of various MOS parameters like body doping concentration, applied drain and substrate biases, the thickness of the thin-film, gate oxide and buried oxide.

- **Threshold Voltage**

A compact, physically threshold voltage model for dual material surrounding gate MOSFET is then derived based on an analytical solution of a 2-D Poisson equation. The model successfully describes the film thickness dependence of the threshold voltage and satisfactorily predicts threshold voltage roll off with decreasing channel lengths. It is shown that Minimum channel potential and consequently $V_{th}$ sensitivity to thin –film thickness of a DMSG is reduced in comparison to a single material Surrounding gate (SMSG). The effect of various MOS parameters like body doping density, applied substrate bias, the thickness of thin film, gate oxide and buried oxide on the threshold voltage can be visualized with the help of the analytical expression.

- **Transconductance to drain current ratio**

Analytical model of the transconductance to drain current ratio is developed based on the surface potential model and the short channel
performance of the proposed DMSG structure is compared with the SMSG MOSFET. The model allows greater flexibility in selecting device parameters as compared to DG and SMSG MOSFETs to achieve the desired $g_m/I_d$ values. The model includes the effect of various MOS parameters like body doping concentration, applied drain source voltages, the thickness of the thin-film, and gate oxide. The developed model will be useful for performance prediction and device structure optimization for realizing future ULSI circuits with DMSG MOSFETs.

- **New Scaling Theory including ECPE effect**

  A general scaling theory for DMSG MOSFET is first derived by solving a 2-D Poisson’s equation in the channel region. Through a concept of effective conducting path effect location, this model provides clear physical explanations of subthreshold swing behavior in short channel DMSG devices and helps identify applicability and limitations of previous models. A compact analytical subthreshold swing expression for DMSG MOSFETs is obtained that yields improved agreement with numerical simulations. A scale length $\lambda$ from the parabolic approximation method and its explicit approximate expressions are derived and readily quantify design requirements for DMSG devices. To limit subthreshold swing roll up with decreasing channel lengths, it is imperative to reduce the silicon thickness and the gate oxide thickness.

- **Two-dimensional simulation studies**

  2-D MEDICI simulations were used to explore and compare the novel attributes offered by the DMSG structure with a conventional SMSG in terms of $V_{th}$ variation with decreasing channel length, drain induce barrier
lowering, leakage current, drive current, and voltage gain. The unique features of the DMSG are: \( V_{th} \) roll-up with decreasing channel length, reduced DIBL and simultaneous transconductance enhancement and SCE suppression. These features can be controlled by a new way of gate material engineering. A gate length ratio of \( L_1/L_2 = 1 \) and a work function difference of \( \Delta W = 0.4 \text{ eV} \) is found to be optimum for both logic and analog applications for a FD DMSG SOI MOSFET.

7.3 SUGGESTIONS FOR THE FUTURE WORK

In this work, a two-dimensional model is presented. The same model can be extended to partially depleted DMSG MOSFETs. Further, the model can be used to determine drain current, capacitance voltage characteristics and small signal parameters. The extracted parameters will be used for development of small model and calculation of Y-parameters, Z-parameters and/or S-parameters in the study of RF device applications. The work can further be extended for three-dimensional (3-D) analysis of DMSG MOSFETs; to explore the potential distribution, electric field distribution, threshold voltage, and subthreshold swing. The use of DMSG MOSFETs in CMOS nanoscale application has become considerable. But with the increase in packing densities, new geometry MOSFET structures must be given a thought.

In addition to this work, a temperature dependent model for nanoscale MOSFETs can be developed. The calculation of model elements like parasitic resistance and capacitance can also be done and further can be included in the model for the calculation of cut-off frequencies and drain current.
A lot of research has already been done for carbon nanotubes but still there are no suitable compact models for the threshold voltage for that device. Also, the strained materials are interesting to be used in SOI multiple gate devices, Such as FINFET and the Compact modeling for those devices is still an open issue.

7.4 CONCLUSION

In this thesis, an attempt has been made to develop 2D models for analyzing surface potential, electric field analysis, threshold voltage, transconductance to drain current ratio, and subthreshold swing for DMSG MOSFETs. The results obtained are better than SMSG MOSFETs. This can be extended for further research.