CHAPTER 6

CONCLUSION

6.1 INTRODUCTION

This thesis investigated the performance of the single parity check (SPC) product code. The structural analysis of the erasure patterns was done. In structural analysis, based on the position of the erasure bits, the erasure patterns are classified into two types namely basic patterns and generated patterns. Based on the number of rows and the number of columns of the occupied erasure bits, the basic pattern is classified into recoverable basic pattern and unrecoverable basic pattern.

The mathematical analysis was done and the numbers of recoverable and unrecoverable basic patterns were found. The method to find the number of patterns generated from the recoverable basic patterns was given. The numerical results of a single parity check product codes of size 16 X 16 for different number of erasures were obtained. Simulation of the post decoding erasure rate was done under three different conditions namely (i) based on minimum distance (ii) based on the condition that all erasure pattern up to five erasures are recoverable and (iii) based on the condition that all erasure patterns generated from the recoverable basic pattern are recoverable.

In the recoverability study of the SPC product code, the algorithm for finding all unrecoverable basic patterns for a given number of erasures was studied. Even though the basic pattern is unrecoverable some of the patterns generated from the unrecoverable basic pattern are recoverable. A detailed mathematical analysis has been carried out and the numbers of recoverable and unrecoverable patterns generated from the unrecoverable basic patterns were found.

The total number of recoverable patterns generated from both recoverable and unrecoverable basic patterns were found. For the unrecoverable patterns generated from the unrecoverable basic pattern, some of the erasures may be recovered. Hence for those patterns, the average number of remaining erasures after decoding was evaluated The various bound on the post decoding erasure rate was studied graphically and the tight upper bound for the post decoding rate was found. It is clearly proved that the error correcting capability of the single parity check product code is extremely good and it is beyond the minimum Hamming distance.

6.2 FUTURE RESEARCH
There are some fruitful ways for future work. The same concept could be extended for multi dimensional SPC product code. Since the mathematical analysis of multi dimensional SPC product codes is very difficult, an efficient algorithm could be developed for finding the various parameters. Further, the analysis of two dimensional SPC product code of higher size (greater than 16 X 16) could be done. This technique could be extended to wireless and mobile environment in the future. Due to the growing demands for real time applications in packet networks, techniques for low delay reliable communications in the presence of bursts are becoming increasingly desirable. Hence a VLSI implementation of hybrid error control scheme for ATM network using SPC product could be developed.

6.3 SUMMARY

This research is mainly focused on the performance of the SPC product code under erasure decoding. The structural analysis of the erasure patterns has been done. A detailed mathematical analysis of the SPC product code has been carried out. The performance of the SPC product code in terms of the post decoding erasure rate was studied. It is found that the performance of the single parity check code is extremely good even though the minimum distance of single parity check code is less.