CHAPTER 3

DESIGN OF LOW IF RECEIVER

3.1 INTRODUCTION

The design of a radio frequency receiver depends primarily on the choice of architecture based on various criteria including complexity, cost, power consumption and the number of external components. Various receiver architectures such as homodyne, heterodyne, low IF and super regenerative structures are commonly available.

The major problem in the homodyne receiver structure is that DC offset voltage gets added at the output of the mixer when the leakage from the local oscillator is mixed with the local oscillator signal itself. This could saturate the successive stages and affect the signal detection process. Since the mixer output is a base band signal, it can easily be corrupted by the large flicker noise of the mixer (Darabi and Abidi 2000) especially when the incoming RF signal is weak.

The drawback of the super regenerative receiver is that it is suitable only for OOK modulation. They suffer from poor selectivity and lack of stability. The super heterodyne architecture overcomes many of the disadvantages of direct conversion and the super regenerative receivers at the expense of an off-chip IF filter and a frequency synthesizer. But the performance of the super heterodyne architecture could only be improved at the expense of power consumption. Thus the low IF architecture has been taken for study.
Since the architecture uses lesser number of components and consumes less power when compared to super heterodyne architecture, it is used in the receiver design. Figure 3.1 shows the architecture of the proposed Low IF Receiver.

![Figure 3.1 Architecture of the proposed Low IF Receiver](image)

3.2 LOW NOISE AMPLIFIER

In WSN transceivers, an LNA is typically the first amplifying stage of the receiver. The low noise amplifier provides input matching and improved isolation for the down converter. It serves as a buffer between the antenna and the down converter stage. In the absence of LNA the 50Ω antenna impedance would directly load the resonant tank which dramatically lowers the Q of the tank circuit (Jia Yi Chen et al 2007). The low noise amplifiers must achieve high gain and moderate noise figure while simultaneously providing input impedance matching. Thus, it is responsible for providing signal amplification without degrading the SNR. Its noise factor sets a lower bound on the noise factor of the entire receiver, which is expressed by the Equation (3.1) as,

\[
F = F_1 + \frac{F_2 - 1}{A_{11}^2} + \frac{F_3 - 1}{\left(\frac{A_{11}}{2}\right) \times A_{12}} + \ldots
\]  

(3.1)
where, $A_{vi}$ represents the voltage gain of the $i^{th}$ block and $F_1$, $F_2$, and $F_3$ are the noise factors of the LNA, mixer and filter respectively (Fris 1944 and Rofougaran 1998). The gain of the LNA has to be large enough to suppress the noise contributions of the successive mixer and base band sections. However, higher gain may overload the mixer which in turn perturbs the receiver linearity.

The LNA must also have sufficient linearity to prevent the intermodulation products of a strong interferer from overwhelming the weak desired signal. Equation (3.2) gives the relationship between the IIP$^3$ of the receiver, LNA, mixer and the filter.

$$\frac{1}{IIP^3_3} = \frac{1}{IIP^3_1} + \frac{A^2_{vi}}{IIP^3_2} + \frac{(A_{v1} \times A_{v2})^2}{IIP^3_3}$$

(3.2)

Also the input impedance of the LNA has to be designed to match the characteristic impedance (50Ω) of the antenna. The output matching is also required if the LNA is followed by an external filter. In addition, the LNA must provide sufficient reverse isolation to reduce the amount of the LO signal that leaks from the mixer to the antenna (Razavi 1998).

Thus the critical benchmark for characterizing the performance of an LNA are the gain, noise figure, power consumption, S-parameters, stability, linearity, ease of input matching and matching accuracy relative to 50Ω impedance.

Table 3.1 shows the popular CMOS LNA architectures available in the literature. It also gives the merits and demerits of using the LNA architectures.
Table 3.1 Popular CMOS LNA architectures available in the literature

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Architectures</th>
<th>Merits</th>
<th>Demerits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Resistive Termination</td>
<td>Input impedance matching is very good</td>
<td>Noise figure is large and more power consumption</td>
</tr>
<tr>
<td>2.</td>
<td>Series / shunt Feedback</td>
<td>Broadband input and output match</td>
<td>Stability issue and isolation problem</td>
</tr>
<tr>
<td>3.</td>
<td>Inductive degeneration</td>
<td>Small noise figure and good narrow band match</td>
<td>Consumes large area</td>
</tr>
<tr>
<td>4.</td>
<td>Common Gate LNA</td>
<td>Easy input match and low power consumption</td>
<td>Large noise figure</td>
</tr>
<tr>
<td>5.</td>
<td>Inductor neutralization</td>
<td>Good reverse isolation</td>
<td>Increased area and stability concern</td>
</tr>
<tr>
<td>6.</td>
<td>Current reuse</td>
<td>High Gain and Low power</td>
<td>External matching network required</td>
</tr>
</tbody>
</table>

In order to reduce the power consumed by the LNA intended for the low power wireless sensor network applications, five novel LNA architectures are proposed. The proposed modified architectures are listed below. They are:

(i) Inductive feedback Common Source LNA
(ii) Series Inductive Resistive feedback Common Source LNA
(iii) Inductive feedback Common Gate LNA
(iv) Series Inductive Resistive feedback Common Gate LNA
(v) Current reuse Inductive feedback LNA

The following section gives the detailed analysis and performance of the architectures proposed above. Each circuit will have its own advantages and disadvantages. A comparative study is carried out for finding out the best low power LNA suitable for the wireless sensor network transceiver.
3.2.1 Inductive Feedback Common Source LNA

A cascode Common Source LNA with inductive feed through has been taken for the study is shown in Figure 3.2. The cascode is generally used in analog designs for two reasons. First, the cascode provides an enhancement of the small signal output resistance over the single-transistor gain stage. Secondly, the cascode also reduces the impact of the so-called Miller capacitor, by reducing the gain across the feedback capacitor of the MOS device.

![Figure 3.2 Single ended inductive feedback CS LNA](image)

The reactive feedback network implemented allows the LNA to operate under low supply voltage. This feedback inductance is able to control the gain, stability and input impedance. Since the LNA uses negative feedback, it provides better stability at the expense of the gain. Also it is obvious that for voltage shunt feedback amplifiers input impedance is lesser when compared to the amplifiers without feedback.
3.2.1.1 Input impedance matching

In the voltage shunt feed back connection, a fraction of the output voltage is fed back to the input through the inductive feed back network. This connection reduces both the input and output impedance of the LNA by a factor \((1 + \beta A)\).

To analyze the input matching network of LNA, the equivalent small signal model of LNA is shown in Figure 3.3. The input impedance \(Z_{in}\) can be derived from the small signal model of the LNA.

The input impedance can be derived as,

\[
Z_{in} = \frac{V_i}{I_i} = \frac{I_1 \times sL_g + \frac{I_1}{sC_{gs1}} + I_s \times sL_s}{I_i} \quad (3.3)
\]

Figure 3.3 Small signal model of inductive feedback CS LNA to calculate \(Z_{in}\)
where, \( V_1 \) is the input voltage, \( I_1 \) is the input current and

\[
I_s = I_1 + g_{m_1} V_{gs_1}
\]  

(3.4)

By substituting the Equation (3.4) in Equation (3.3) leads to,

\[
I_1 \left( sL_g + \frac{1}{sC_{gs_1}} \right) + \left( I_1 + g_{m_1} V_{gs_1} \right) sL_s = \frac{I_1}{I_1}
\]  

(3.5)

But,

\[
V_{gs_1} = \frac{I_1}{sC_{gs_1}}
\]  

(3.6)

Hence the Equation (3.5) can be rewritten as,

\[
I_1 \left( s(L_g + L_s) + \frac{1}{sC_{gs_1}} \right) + g_{m_1} \left( I_1 \frac{I_1}{sC_{gs_1}} \right) sL_s = \frac{I_1}{I_1}
\]  

(3.7)

\[
I_s(L_g + L_s) + I_1 \left( \frac{1}{sC_{gs_1}} + g_{m_1} \frac{L_s}{C_{gs_1}} \right) = \frac{I_1}{I_1}
\]  

(3.8)

By rearranging the above Equation (3.8) leads to,

\[
I_1 \left( s(L_g + L_s) + \left( \frac{1}{sC_{gs_1}} + g_{m_1} \left( \frac{L_s}{C_{gs_1}} \right) \right) \right) = -\frac{I}{I_1}
\]  

(3.9)

\[
= s(L_g + L_s) + \left( \frac{1}{sC_{gs_1}} + g_{m_1} \left( \frac{L_s}{C_{gs_1}} \right) \right)
\]  

(3.10)
By considering the real part of the impedance from the Equation (3.10),

\[ Z_{in} = \frac{g_{m}}{C_{gs}} L_s \]  \hspace{1cm} (3.11)

\[ = \omega_T L_s \]  \hspace{1cm} (3.12)

where,

\[ \omega_T = \frac{g_m}{C_{gs}} \]  \hspace{1cm} (3.13)

At the series resonance of the input circuit, the impedance is purely real and proportional to \( L_s \). If \( f_T = 2.4 \text{GHz} \), a 50\( \Omega \) impedance requires only 3.3nH for \( L_s \). This small amount of inductance can easily be obtained with a single bond wire or on chip spiral inductor.

Since ‘\( Z_{in} \)’ is to be matched to 50\( \Omega \) impedance,

\[ \text{Re}\{Z_{in}\} = \left( \frac{g_m}{C_{gs}} \right) L_s = R_s = 50\Omega \]  \hspace{1cm} (3.14)

Normally an inductor ‘\( L_g \)’ is added in series with the gate. It is designed so that at the resonant frequency it cancels out \( C_{gs} \). \( L_g \) is used to set the resonant frequency once \( L_s \) is chosen to satisfy the criterion of a 50 \( \Omega \) input impedance. That is,

\[ \text{Im}\{Z_{in}\} = \omega L_s - \frac{1}{\omega C_{gs}} = 0 \]  \hspace{1cm} (3.15)
3.2.1.2 Noise Figure analysis

The small signal model of the inductively degenerated cascode Common Source inductive feed through LNA is shown in Figure 3.4. It is considered here for noise analysis and the parameters $C_{gd}$ and $g_{mb}$ of the transistors are ignored for simplicity.

![Small signal equivalent circuit of the inductive feedback CS LNA for noise analysis](image)

Figure 3.4 Small signal equivalent circuit of the inductive feedback CS LNA for noise analysis

The capacitor $C_x$ represents all the parasitic capacitances at node ‘x’, which can be estimated by the Equation (3.16) as,

$$C_x = C_{gs2} + C_{sb2} + C_{db1}$$  \hspace{1cm} (3.16)

where, $C_{gs2}$ is the gate source capacitance of the transistor M2

$C_{sb2}$ is the source bulk capacitance of the transistor M2

$C_{db1}$ is the drain bulk capacitance of the transistor M1

Normally the parasitic capacitance $C_x$ reduces the gain of the first stage and hence increases the noise factor of the LNA.
The effective transconductance of the input stage is defined by the Equation (3.17) as,

\[ G_{m_{\text{eff}}} = \frac{I_{\text{out}}}{V_{i}} = Q_{m\text{in}}g_{m} \]  \hspace{1cm} (3.17)

The effective ‘Q’ of the amplifier input circuit is given by,

\[ Q_{m\text{in}} = \frac{1}{\omega_{o}C_{p_{1}}(R_{s} + \omega_{f}L_{s})} \]  \hspace{1cm} (3.18)

where, \( R_{s} \) is the input source resistance.

By substituting Equation (3.18) in Equation (3.17) leads to,

\[ G_{m_{\text{eff}}} = \frac{g_{m}}{\omega_{o}C_{p_{1}}(R_{s} + \omega_{f}L_{s})} \]  \hspace{1cm} (3.19)

At the series resonance of the input circuit, the input impedance \( Z_{\text{in}} \) is purely real and is proportional to \( L_{s} \). By using the Equation (3.13), Equation (3.19) can be rewritten as,

\[ G_{m_{\text{eff}}} = \frac{\omega_{f}}{2\omega_{o}R_{s}} \]  \hspace{1cm} (3.20)

The output noise power density due to the 50\( \Omega \) source is,

\[ \overline{V_{o,R_{s}}} = 4kTR_{s}G_{m_{\text{eff}}}^{2} \]  \hspace{1cm} (3.21)

In a similar fashion, the power density due to \( R_{g} \) can be expressed as,

\[ \overline{V_{o,R_{g}}} = 4kTR_{g}G_{m_{\text{eff}}}^{2} \]  \hspace{1cm} (3.22)
The dominant noise contributor internal to the LNA is the channel current noise of the first MOS device. By using the Equation (A1.9) given in Appendix 1, the output noise power density arising from this source is,

\[
\overline{V_{o_{\Delta d}}} = \frac{4kT\gamma g_{d0}}{\left(1 + \frac{\omega_r L_s}{R_i}\right)^2}
\]

\[= kT\gamma g_{d0}
\]

(3.23)

(3.24)

Using the Equations from (3.21) to (3.24) the noise figure is derived as,

\[
NF = \frac{4kTR G_{m_d}^2 + 4kTR G_{m_d}^2 + kT\gamma g_{d0}}{4kTR G_{m_d}^2}
\]

\[= 1 + \frac{R_s}{R_g} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_r}\right)^2 + 4R_s \gamma_2 g_{d0} \left(\frac{\omega_0^2 C_x}{\omega_r g_{m2}}\right)^2
\]

(3.25)

(3.26)

The above Equation (3.26) reveals several important features of the LNA. The third term \(\gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_r}\right)^2\) arising from channel thermal noise dominates the noise figure performance. According to this expression, a reduction of \(g_{d0}\) without modifying \(\omega_r\) means improvement of noise figure and reduction of power consumption. This result can be achieved by scaling down the width of the MOS transistor while maintaining constant bias voltages on its terminals and without changing the channel length. The last term \(4R_s \gamma_2 g_{d0} \left(\frac{\omega_0^2 C_x}{\omega_r g_{m2}}\right)^2\) arises due to the effect of the cascode transistor M2.
3.2.1.3 Voltage Gain

The gain is calculated using the relation,

\[
Gain(dB) = 20\log \left( \frac{V_o}{V_{in}} \right)
\]  \hspace{1cm} (3.27)

In order to increase the gain, one can introduce a constant current source at the source leg and is shown in Figure 3.5.

![Inductive feedback Common Source LNA using constant current source](image)

Figure 3.5 Inductive feedback Common Source LNA using constant current source

3.2.1.4 Differential mode Inductive Feedback CS LNA

There are several advantages in using a differential design. Firstly, the virtual ground formed at the tail removes the sensitivity to parasitic ground inductances. Secondly, the differential amplification of the signal ensures attenuation of the common mode signal. In most of the systems the
common mode signal will be noise. Thirdly, the use of Gilbert mixers and image rejection schemes require to be fed from a differential source. Hence the differential mode LNA is preferred. The structure is shown in Figure 3.6.

![Figure 3.6 Differential mode inductive feedback CS LNA](image)

3.2.1.5 Performance Evaluation

For this study the normalized energies at 1.2V are based on simulations and these are extrapolated over a range of $V_{dd}$ using fundamental analytical models. A lower $V_{dd}$ also reduces the electric fields in the device and improves its long term reliability. However, reduction of $V_{dd}$ limits the dynamic range of the ADC and reduction of the voltage headroom needed for the cascode transistors in analog/RF circuits.
An inductive feed back LNA topology, implemented in 120nm CMOS technology intended for wireless sensor networks is simulated using ORCAD 9.2. The reactive feed back network implemented allows the LNA to operate under low supply voltage. In addition to stabilize the gain and noise figure, the feed back network enables input and output matching. Figure 3.7 shows the FFT of the output at 2.4GHz. At this frequency the LNA achieves a gain of 20dB. Figure 3.8 shows the output voltage of the inductive feedback Common Source LNA at different frequencies.

Figure 3.7 FFT of the output of single ended inductive feedback CS LNA

Figure 3.9 shows the gain at various frequencies. The gain can be increased by increasing the value of the constant current source.
Figure 3.8  Output voltage of inductive feedback CS LNA at various frequencies

Figure 3.9  Variation in Gain of inductive feedback CS LNA at various frequencies
Figure 3.10 shows the simulated input noise and the output noise voltages for the single ended common source LNA at 27°C. From the graph the noise figure is calculated as 3.81 dB. When compared to the Common Gate LNA, the noise figure of the Common Source LNA is less. In CS LNA, the input impedance matching is achieved with the noiseless components, hence it achieves lower noise figure.

![Graph showing input and output noise voltages for inductive feedback CS LNA at various frequencies.](image)

**Figure 3.10** Input Noise voltage and Output noise voltage of inductive feedback CS LNA at various frequencies

The power consumed by the LNA is plotted in Figure 3.11 for various supply voltages operated at 2.4GHz. Since the sensor network is required to operate at hostile temperatures, the performance is evaluated at different temperatures also. The power consumption by the LNA at various supply voltages ranging from 1V to 2V and at different temperatures is shown in Figure 3.12.

Similarly the performance evaluation is done for finding out the small signal gain at different supply voltages when operated at 2.4GHz is presented in Figure 3.13.
Figure 3.11 Power Consumption versus supply voltage of inductive feedback CS LNA at 2.4 GHz

Figure 3.12 Temperature versus Power Consumption of inductive feedback CS LNA at various supply voltages
Figure 3.1 Gain versus frequency of inductive feedback CS LNA at various supply voltages

The linearity of the proposed LNA is checked using two tones at 2.4GHz and 2.42GHz. The input referred third order intercept point IIP₃ is found from the Figure 3.14 as -3.1dBm.

Figure 3.14 Input power versus Output power of inductive feedback CS LNA at 2 tones
Scattering refers to the way in which the traveling currents and voltages in a transmission line are affected when they meet a discontinuity caused by the insertion of a component into the transmission line. This is equivalent to the wave meeting impedance differing from the line's characteristic impedance. Thus the S parameters are to be analyzed. Figures 3.15 and 3.16 show the scattering performances of the proposed LNA. From the simulations it is found that $S_{11}$ is $<-12dB$ which is an acceptable impedance match over the range of frequencies. The power gain $S_{21}$ is around 20dB from 1.5 to 4GHz frequencies.

![Figure 3.15 S11 of inductive feedback CS LNA at various frequencies](image)

**Figure 3.15** $S_{11}$ of inductive feedback CS LNA at various frequencies
Figure 3.16 $S_{21}$ of inductive feedback CS LNA at various frequencies

A summary of the performance of the CMOS LNA is tabulated in Table 3.2. The evaluation is done at $27^\circ C$.

Table 3.2 Simulated performance of single ended inductive feedback CS LNA at $27^\circ C$

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Single ended inductive feedback CS LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply voltage ($V_{dd}$)</td>
<td>1.2V</td>
</tr>
<tr>
<td>LNA Voltage Gain</td>
<td>20.34dB</td>
</tr>
<tr>
<td>LNA Noise figure</td>
<td>3.81dB</td>
</tr>
<tr>
<td>$IIP_3$</td>
<td>-3.1dBm</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>&lt;-12dB</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>20dB</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>Power consumed by the LNA</td>
<td>32.26µW</td>
</tr>
<tr>
<td>Technology</td>
<td>120nm CMOS</td>
</tr>
</tbody>
</table>
3.2.2 Series Inductive Resistive Feedback CS LNA

At low frequencies the phase of $S_{21}$ is around $180^\circ$. As the frequency increases the phase of $S_{21}$ starts to approach towards $90^\circ$, which creates undesirable positive feedback conditions. This means that a portion of the output signal will add in phase with the input signal, causing an increase in gain and forces the amplifier into instability. To alleviate this problem, the amount of feedback can be reduced as the feedback increases and as the phase of $S_{21}$ approaches $90^\circ$. A typical method to achieve the reduction in the feedback is to add an inductor in series with the shunt feedback element (Radmanesh 2001). Figure 3.17 shows the series inductive resistive feedback LNA.

![Series Inductive Resistive Feedback LNA Diagram](image)

**Figure 3.17 Single ended series inductive resistive feedback CS LNA**

Figure 3.18 is a simplified small signal model of the series inductive resistive feedback CS LNA.
Figure 3.18 Small signal equivalent circuit of the series inductive resistive feedback CS LNA

The input impedance of the LNA ‘Z<sub>in</sub>’ can be derived by recalling the Equation (3.10) as,

\[
Z_{in} = s \left( L_g + L_s \right) + \left( \frac{1}{s C_{gs}} + g_m \left( \frac{L_s}{C_{gs}} \right) \right)
\]  

(3.28)

In the Equation (3.28), the real part of ‘Z<sub>in</sub>’ is to be matched to 50Ω impedance by assuming the imaginary part as zero.

In the voltage shunt feedback connection, a fraction of the output voltage is fed back to the input through the inductive resistive feed back network. In order to increase the gain, constant current source is provided at the source leg as shown in Figure 3.19.
Since the front end of the receivers use the differential mode LNAs it is considered for analysis. Figure 3.20 depicts the series inductive resistive feed back differential mode CS LNA.
3.2.2.1 Performance Evaluation

Figure 3.21 shows how the power consumed by the circuit varies with respect to supply voltages.

Figure 3.22 shows the FFT of the output of the single ended series inductive resistive feedback CS LNA at 2.4GHz. At this frequency the LNA achieves a gain of 18.79dB. Figure 3.23 shows the frequency response of the proposed LNA. The gain can be increased further by increasing the value of the constant current source.

Figure 3.21  Power consumption versus supply voltage of series inductive resistive feedback CS LNA
Figure 3.22 FFT of the output of the series inductive resistive feedback CS LNA

Figure 3.23 Gain versus frequency of series inductive resistive feedback CS LNA
Figures 3.24 to 3.27 show the simulated input noise and the output noise voltages for the single ended series inductive resistive feed back common source LNA at 27° C. From the graphs, the noise figure is calculated as 3.45 dB.

**Figure 3.24**  Input noise voltage of series inductive resistive feedback CS LNA at various frequencies

**Figure 3.25**  Input rms noise voltage of series inductive resistive feedback CS LNA at various frequencies
Figure 3.26 Output noise voltage of series inductive resistive feedback CS LNA at various frequencies

Figure 3.27 Output rms noise voltage of series inductive resistive feedback CS LNA at various frequencies
The simulated S parameters of the LNA are shown in Figures 3.28 and 3.29. From the simulations it is found that $S_{11}$ is $<-15$dB which is an acceptable impedance match over the range of frequencies. The power gain $S_{21}$ is around 19dB over the frequencies ranging from 1.5 to 3.5GHz.

![Figure 3.28 $S_{11}$ of series inductive resistive feedback CS LNA at various frequencies](image1)

![Figure 3.29 $S_{21}$ of series inductive resistive feedback CS LNA at various frequencies](image2)
At 2.4GHz frequency, the proposed LNA consumes a total power of 2.88mW from 1.2V supply. It provides a gain of 18.79dB and the noise figure of 3.45dB.

The LNA linearity is normally dominated by the voltage to current conversion transistor $M_1$. If the voltage gain of $M_2$ is greater than one, then the linearity of $M_1$ plays an important role. Linearity is checked using two tones at 2.4GHz and 2.42GHz. The input referred third order intercept point $IIP_3$ is calculated from the Figure 3.30 is -2.88dBm. A summary of the performance of the proposed series inductive resistive feedback CS LNA is tabulated in Table 3.3.

![Figure 3.30 Input power versus Output power of series inductive resistive feedback CS LNA at 2 tones](image)

Table 3.3

<table>
<thead>
<tr>
<th>Output power (dBm)</th>
<th>Input power (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-80</td>
<td>0</td>
</tr>
<tr>
<td>-70</td>
<td>-10</td>
</tr>
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<td>-70</td>
</tr>
<tr>
<td>0</td>
<td>-80</td>
</tr>
</tbody>
</table>

$IIP_3=-2.88$dBm
Table 3.3  Simulated performance of the single ended series inductive resistive feedback CS LNA at 27°C

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Single ended series inductive resistive feedback CS LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply Voltage (V_{dd})</td>
<td>1.2V</td>
</tr>
<tr>
<td>LNA Voltage Gain</td>
<td>18.79dB</td>
</tr>
<tr>
<td>LNA Noise Figure</td>
<td>3.45dB</td>
</tr>
<tr>
<td>Power consumed by the LNA</td>
<td>2.88mW</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>S_{11}</td>
<td>&lt;-15dB</td>
</tr>
<tr>
<td>S_{21}</td>
<td>19dB</td>
</tr>
<tr>
<td>IIP₃</td>
<td>-2.88dBm</td>
</tr>
<tr>
<td>Technology</td>
<td>120nm CMOS</td>
</tr>
</tbody>
</table>

3.2.3  Inductive Feedback Common Gate LNA

3.2.3.1 Theory and analysis of CG LNA

The NF_{min} of Common Source LNA tends to grow up as the operating frequency increases. So the Common Gate LNA topology shown in Figure 3.31 is adopted due to the two main reasons. Firstly, the minimum achievable noise figure for Common Gate LNA possesses a relatively flat spectrum. Secondly, it consumes less power compared to the common source LNA.
There are various ways to implement gain control for LNA, such as biasing, current steering, configurable load impedance and shunt feedback. In this work, the feedback path has been modified using an inductive shunt feedback to control the gain, stability and input impedance. The reactive feedback loop around the output lowers the next stage input impedance while compensating for inter-stage attenuation losses. A negligible DC loss with a reactive feedback also allows the circuit to operate under low supply voltage, which further reduces the DC power consumption (Masato Koutani et al 2007). This allows the operation from a single 1.2V supply that can be shared with the digital base band circuitry.

Table 3.4 gives the advantages (+) and disadvantages (-) of CS and CG LNA stages (Zhuo et al 2005). It clearly indicates that the Common Gate LNA topology is more attractive if its effective $g_m$ is increased and its noise figure is decreased.
Table 3.4 Comparison of Common Source and Common Gate LNA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CS LNA</th>
<th>CG LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>$G_{\text{meff}}$</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Parasitic Sensitivity</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Input matching</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>D.C power</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>

As cited by Zhuo et al (2005) if the $G_{\text{meff}}$ is boosted independently by modifying its input matching conditions, then the noise factor of the CG LNA can be reduced. This is accomplished in the proposed circuit, wherein inverting amplification ‘A’ is introduced between the source and gate terminals so that $G_{\text{meff}}=(1+A)g_m$. The resulting increase in the transconductance brings two significant improvements to the CG LNA topology. It reduces noise factor as well as power consumption by the same factor.

3.2.3.2 Noise Figure analysis

Figure 3.32 shows the small signal equivalent circuit of the proposed inductive feedback CG LNA including the thermal noise of the load and the FET internal noise sources $v_n$ and $i_n$. They are treated as independent noise sources and the superposition theorem is used to determine the total output noise. In the equivalent circuit, $g_{m1}$ and $g_{m2}$ represents the transconductance of the transistors $M_1$ and $M_2$ respectively. $g_{mb1}$ and $g_{mb2}$ are the back gate transconductance of the transistors $M_1$ and $M_2$. $R_{g1}$, $R_{g2}$ are the
gate resistance of the transistors, $\frac{i_{n,d}^2}{2}$, $\frac{i_{n,g}^2}{2}$ are the transistor thermal noise source and the induced gate noise source respectively.

![Figure 3.32 Small signal Equivalent circuit of the proposed inductive feedback CG LNA](image)

The analysis of the CG LNA starts with the study of the four noise parameters. In order to find out the noise factor of the CG LNA, the four noise parameters $R_n$, $G_0$, $B_0$ and $F_{\text{min}}$ are considered. The four noise parameters can be determined by $v_n$, $i_n$, $G_r$ and $B_r$ by the transformation rules given in Rothe et al (1956), Haus (1960), Chih Fan Liao and Shen Iuan Liu (2007), Jarkko Jussila and Pete Sivonen (2008). The noise voltage $v_n$ and the noise current $i_n$ are characterized by correlation admittance $Y_r$ ($Y_r = G_r + jB_r$), where $G_r$ and $B_r$ are the real and imaginary parts of $Y_r$ respectively. $G_0$ and $B_0$ are the real and imaginary parts of the optimum source admittance $Y_0$. $R_n$ is the equivalent noise resistance which characterizes the sensitivity of noise factor $F$.

The following noise parameters for the proposed inductive feed through CG LNA are derived in the Appendix 2. These parameters
represented by the Equations (3.29) to (3.34) are useful for calculating the noise figure of the LNA.

The equivalent noise resistance \( R_n \) is derived as

\[
R_n = \frac{\gamma_1 g_{m1} + \frac{1}{(R_f + j\omega L_f)}}{\left( g_{m1} + \frac{1}{(R_f + j\omega L_f)} \right)^2} \quad (3.29)
\]

For the inductive feedback CG LNA \( G_0 \) is derived as,

\[
G_0 = \omega C_{gs} \sqrt{\frac{\delta}{5\gamma_1}} \left( 1 - |C|^2 \frac{\gamma_1 g_{m1}(R_f + j\omega L_f)}{1 + \gamma_1 g_{m1}(R_f + j\omega L_f)} \right) \frac{\gamma_1(1 + g_{m1}(R_f + j\omega L_f)^2)}{g_{m1}(R_f + j\omega L_f)(1 + \gamma_1 g_{m1}(R_f + j\omega L_f))} \quad (3.30)
\]

Both the thermal noise and the induced gate noise of the transistor originate from the same source, but they are partially correlated with a complex coefficient \( C \), which is given by the Equation (3.31) as,

\[
C = \frac{I_{n.g}^* I_{n.d}^2}{\sqrt{I_{n,g}^2 I_{n,d}^2}} \quad (3.31)
\]

The imaginary part of correlation admittance \( B_r \) is derived as,

\[
B_r = \omega C_{gs} \left[ 1 + \frac{\gamma_1 \left( 1 + g_{m1}(R_f + j\omega L_f) \right)}{1 + \gamma_1 g_{m1}(R_f + j\omega L_f)} \right] \frac{|C|}{\sqrt{\frac{\delta}{5\gamma_1}}} \quad (3.32)
\]

and

\[
B_0 = -B_r \quad (3.33)
\]
Due to the existence of the parasitic capacitance \( C_x \), the noise figure of the CG LNA is influenced by the cascade transistor \( M_2 \). By considering the effect of the cascode transistor, the minimum noise factor of the proposed CG LNA will be derived as,

\[
F_{\text{min}} = 1 + 2 \left( \frac{\omega_0}{\omega_T} \right) \frac{\tilde{\gamma}_T}{5} \left[ 1 - \left( \frac{\omega_0}{\omega_T} \right)^2 \frac{g_{\text{de}}(R_f + j\omega L_f)}{1 + \gamma g_{\text{m}}(R_f + j\omega L_f)} \right] \frac{g_{\text{m}}(R_f + j\omega L_f)(1 + \gamma' g_{\text{m}}(R_f + j\omega L_f))}{\gamma' \left( 1 + g_{\text{m}}(R_f + j\omega L_f)^2 \right)} + 4 R_s \gamma' g_{\text{de}} \left( \frac{\omega_0^2 C_x}{\omega_T g_{\text{m}}^2} \right) \]

(3.34)

The third term in the Equation (3.34) represents the factor influenced by the cascade transistor \( M_2 \). The expression for the noise figure as given by the classical noise theory will be (Lee 2004),

\[
F = F_{\text{min}} + \frac{R_s}{G_s} \left[ (G_s - G_o)^2 + (B_s - B_o)^2 \right]
\]

(3.35)

Equation (3.35) is useful for calculating the noise figure of the proposed CG LNA theoretically using the noise parameters represented by the Equations (3.29) to (3.34). For short channels, typical values of \( \gamma \) are 2-3. Therefore typical values of NF will be from 3 to 4dB. The load on the drain determines the bandwidth of the amplifier.

### 3.2.3.3 Voltage Gain

The gain is calculated using the Equation (3.36) and is found as 21.28dB.

\[
Gain(dB) = 20 \log \left( \frac{V_o}{V_i} \right)
\]

(3.36)
For a resistive load, the gain can be calculated using the relation (3.37).

\[ A_v = g_m R_L \]  

(3.37)

For a narrow band design (with potentially more gain) \( R_L \) is to be replaced by an inductor and the gain can be calculated using the Equation (3.38).

\[ A_v = \frac{g_m Q_{Load}}{C 2\pi f_0} \]  

(3.38)

### 3.2.3.4 Input impedance matching

The input impedance for the inductive feedback CG LNA is derived as,

\[
Z_{in} = \left[ 1 + g_m \left( R_f + j\omega L_f \right)(1 + \chi) \right]^{-1} \left( R_f + j\omega L_f + R_L + \eta(\omega_o)g_m \right)
\]

(3.39)

where,

\[
\eta(\omega_o) = \frac{g_f}{g_m} \sqrt{\frac{\alpha}{5}} \left( \frac{\omega_o}{\omega_f} \right)^2
\]

(3.40)

Since the value of \( R_f \) in the Equation (3.39) is very low, the input impedance is approximated as,

\[ Z_{in} = R_{in} = \frac{1}{g_m} \]

(3.41)

Hence in the Equation (3.41), if \( R_{in} = 50\Omega \), then the value of \( g_m = 1/50 = 20\text{mS} \). With the required value of ‘\( g_m \)’ the (W/L) ratio can be determined from the following Equation (3.42) as,

\[ g_m = \sqrt{\frac{2K_i}{I_o} \frac{W}{L}} \]

(3.42)
3.2.3.5 Scattering parameters

Scattering parameter ‘$S_{11}$’ can be proved theoretically by deriving the following Equation (3.43) as,

$$S_{11} = \frac{(R_f + j\omega L_f) + R_L - R_i - g_m R_s (R_f + j\omega L_f)}{(R_f + j\omega L_f) + R_L + R_i + g_m R_s (R_f + j\omega L_f)}$$

(3.43)

The value of the feedback resistance ‘$R_f$’ associated with the feedback inductance is very less, hence $S_{11}$ can be rewritten as,

$$S_{11} = \frac{(j\omega L_f) + R_L - R_i - g_m R_s (j\omega L_f)}{(j\omega L_f) + R_L + R_i + g_m R_s (j\omega L_f)}$$

(3.44)

3.2.3.6 Differential mode Inductive Feedback CG LNA

When compared to the single ended LNA, the differential LNA gives better performance in wireless applications, but it consumes a power of 0.659µW at the same frequency. Figure 3.33 shows the circuit diagram of a differential mode inductive feedback Common Gate LNA.

Figure 3.33 Differential mode inductive feedback CG LNA
3.2.3.7 Performance Evaluation

An inductive feedback CG LNA topology (both single ended and differential mode) implemented in 120nm CMOS technology intended for wireless sensor networks was simulated using ORCAD 9.2. The reactive feedback network implemented allows the LNA to operate under a low supply voltage. In addition to stabilize the gain and noise figure the feedback network enables input and output impedance matching.

Figure 3.34 shows the FFT of the output at 2.4GHz. At this frequency the LNA achieves a gain of 21.4dB. The simulation is performed to obtain the frequency response and its performance against various values of supply voltages. The responses are plotted in Figures 3.35 and 3.36.

![Figure 3.34 FFT of the output of single ended inductive feedback CG LNA](image-url)
Figure 3.35  Small signal gain versus various supply voltage of inductive feedback CG LNA at 2.4GHz

Figure 3.36  Small signal Gain versus frequency of inductive feedback CG LNA at various supply voltages

Figures 3.37 to 3.39 show the simulated input noise and the output noise voltages for the single ended LNA at various temperatures. From the graphs the noise figure was calculated as 4.5dB at 2.4GHz. When compared
to the Common Source LNA the noise figure of the Common Gate LNA is quite high. But the power consumed by the CG LNA is very low, hence it is suitable for low power WSN applications.

Figure 3.37 Input noise voltage of inductive feedback CG LNA at 27°C

Figure 3.38 Output noise voltage of inductive feedback CG LNA at 27°C
In order to extend the life time of the sensor networks, the power consumed by the sensor nodes should be minimized. Since the dominant component of power consumption in CMOS transceiver circuits varies proportionally the square of the supply voltage, significant saving in power consumption can be obtained from the operation at a reduced supply voltage.

The proposed CG LNA was simulated for various supply voltages and the power consumed by the circuit is plotted in Figure 3.40. As the sensor network is required to operate at hostile temperatures, the performance is evaluated at different temperatures. Figure 3.41 illustrates the performance of CGLNA at various temperatures vis-a-vis power consumption at various supply voltages ranging from 0.5V to 1.75V. The noise figure can also be found at various temperatures using the input and output noise voltages.
Figure 3.40  Power consumption versus supply voltage $V_{dd}$ of inductive feedback CG LNA

Figure 3.41 Temperature versus power consumption of inductive feedback CG LNA at various supply Voltages

The third order input intercept point ($IIP_3$) for CG LNA is obtained from the Figure 3.42 as -5.1dBm.
Figures 3.43 and 3.44 show $S_{11}$ and $S_{21}$ performance and it is found that $S_{11}$ is $<-10\text{dB}$ which is an acceptable impedance match over the range of frequencies of interest. The power gain $S_{21}$ is around 20dB from 1.5 to 4GHz frequencies. It is worth noting that the gain of the common gate topology can be increased by increasing the load due to the input matching constraint. The performance of the CGLNA is summarized in Table 3.5.

**Figure 3.42** Input power versus Output power of inductive feedback CG LNA at 2.4GHz

**Figure 3.43** $S_{11}$ of inductive feedback CG LNA at various frequencies
Figure 3.44 $S_{21}$ of inductive feedback CG LNA at various frequencies

Table 3.5 Simulated performance of the single ended inductive feedback CG LNA at 27°C

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Single ended inductive feedback CG LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply voltage ($V_{dd}$)</td>
<td>1.2V</td>
</tr>
<tr>
<td>LNA Voltage Gain</td>
<td>21.28dB</td>
</tr>
<tr>
<td>LNA Noise figure</td>
<td>4.51dB</td>
</tr>
<tr>
<td>Power consumed by the LNA</td>
<td>0.342μW</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>&lt;-10dB</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>20dB</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>Technology</td>
<td>120nm CMOS</td>
</tr>
</tbody>
</table>
3.2.4 Series Inductive Resistive Feedback Common Gate LNA

Figures 3.45 and 3.46 show the single ended and differential mode series inductive resistive feedback Common Gate LNAs. The LNA is simulated at 2.4GHz frequency using 1.2V supply.

Figure 3.45 Single ended inductive resistive feedback Common Gate LNA

Figure 3.46 Differential mode inductive resistive feedback CG LNA
3.2.4.1 Performance Evaluation

The LNA is simulated and the performance is tabulated in the Table 3.6. From the table it is observed that the LNA consumes 1.02mW of power at 2.4GHz frequency. It gives a voltage gain of 15.69dB and a noise figure of 4.09dB.

Table 3.6 Simulated performance of the single ended series inductive resistive feedback CG LNA at 27°C.

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Single ended series inductive resistive feedback CG LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply voltage (V_{dd})</td>
<td>1.2V</td>
</tr>
<tr>
<td>LNA Voltage Gain</td>
<td>15.69dB</td>
</tr>
<tr>
<td>LNA Noise figure</td>
<td>4.09dB</td>
</tr>
<tr>
<td>Power consumed by the LNA</td>
<td>1.02mW</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>Technology</td>
<td>120nm CMOS</td>
</tr>
</tbody>
</table>

Apart from the common gate and common source LNAs, current reuse LNA is also useful for obtaining less power consumption. Hence in this work, a modified inductive feedback LNA using current reuse technique is proposed.

3.2.5 Current reuse Inductive Feedback LNA

The current reuse technique is basically intended to reduce the power consumption by increasing the amplifier’s transconductance (Inui et al 2007). In this work a feedback path has been provided using a shunt inductive element ‘L_{f}’ as shown in Figure 3.47.
The circuit uses cascode topology, which is often used to increase the output impedance by a factor of $g_m r_0$ where $g_m$ and $r_0$ are the transconductance and the drain source resistance of the cascode transistor. But it does not increase the gain of the amplifier because the load impedance is always limited to a lower value at high frequencies.

An improvement of the gain requires revision of the function of the Common Gate transistor. Thus, a new cascode circuit with inductive feedback shown in Figure 3.47 is proposed, where the effective transconductance of the Common Gate transistor is increased resulting in the boosting of gain. Figure 3.48 shows the differential mode inductive feedback Current reuse LNA.

![Figure 3.47 Single ended inductive feedback Current reuse LNA](image)
Figure 3.48 Differential mode inductive feedback Current reuse LNA

3.2.5.1 Performance Evaluation

Simulations are carried out in order to find out the critical parameters of the LNA such as gain, power consumption and noise figure. Figure 3.49 illustrates the voltage gain in dB for the supply voltage ranging from 0.1 to 1.75V. It is clear that as supply voltage increases, gain improves considerably.
Figure 3.49 Small signal forward gain versus supply voltage of inductive feedback Current reuse LNA at 2.4GHz

Figure 3.50 shows the variation in power consumption vis-a-vis variation in supply voltage. The noise figure performance of the LNA is shown in Figures 3.51, 3.52 and 3.53. From the response the noise figure at 2.4GHz is calculated as 1.55dB.

Figure 3.50  Power consumption versus supply voltage $V_{dd}$ of inductive feedback Current reuse LNA
Figure 3.51  Input noise voltage of the inductive feedback Current reuse LNA at different temperatures

Figure 3.52  Output noise voltage of the inductive feedback Current reuse LNA at different temperatures
Figure 3.53  Input and Output noise voltage of the inductive feedback Current reuse LNA at various frequencies

The performance is summarized in Table 3.7. From the table it is seen that noise figure of the LNA is considerably improved when compared to the other proposed LNAs.

Table 3.7 Simulated performance of the inductive feedback Current reuse LNA at 27°C.

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Single ended Current reuse LNA</th>
<th>Differential mode Current reuse LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply voltage (V_{dd})</td>
<td>1.2V</td>
<td>1.2V</td>
</tr>
<tr>
<td>LNA Voltage Gain</td>
<td>17.50dB</td>
<td>17.50dB</td>
</tr>
<tr>
<td>LNA Noise figure</td>
<td>1.55dB</td>
<td>1.55dB</td>
</tr>
<tr>
<td>Power consumed by the LNA</td>
<td>1.8µW</td>
<td>2.70µW</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
<td>50Ω</td>
</tr>
<tr>
<td>Technology</td>
<td>120nm CMOS</td>
<td></td>
</tr>
</tbody>
</table>
3.2.6 Performance Comparison of the proposed CS and CG LNAs

A comparison is done between the proposed Common Source and Common Gate LNAs. Simulations and the theoretical analysis have shown that the common gate LNA with inductive feedback can give astonishingly reduced power consumption for the normalized supply voltage of 1.2V at 2.4GHz frequency. A summary of the performance of the proposed CMOS LNA is tabulated in Table 3.8.

Table 3.8 Simulated performances of single ended LNAs proposed in this work

<table>
<thead>
<tr>
<th>Circuit Schematic</th>
<th>Common Source LNA</th>
<th>Common Gate LNA</th>
<th>Current reuse LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shunt Feedback elements used</td>
<td>L1</td>
<td>Rf</td>
<td>L1</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
<td>2.4GHz</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Supply voltage (Vdd)</td>
<td>1.2V</td>
<td>1.2V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>20.34dB</td>
<td>18.79dB</td>
<td>21.4dB</td>
</tr>
<tr>
<td>Noise figure</td>
<td>3.81dB</td>
<td>3.45dB</td>
<td>4.51dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>32.26μW</td>
<td>2.88mW</td>
<td>0.342μW</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50Ω</td>
<td>50Ω</td>
<td>50Ω</td>
</tr>
<tr>
<td>S11</td>
<td>&lt;-12dB</td>
<td>&lt;-15dB</td>
<td>&lt;-10dB</td>
</tr>
<tr>
<td>S21</td>
<td>20.34dB</td>
<td>18.79dB</td>
<td>21.4dB</td>
</tr>
</tbody>
</table>

The evaluation is done at 27°C. Here, the CG LNA with inductive feedback circuit is selected as the analog front end of the transceiver in wireless sensor nodes.

3.2.7 Performance Comparison of LNAs reported in the Literature

Table 3.9 shows the performance comparison of LNA designs reported in the recent literature.
Table 3.9 Performance Comparison of proposed LNAs with the LNAs reported in the Literature

<table>
<thead>
<tr>
<th>References</th>
<th>Frequency (GHz)</th>
<th>Supply Voltage $V_{dd}$ (V)</th>
<th>Power Consumption (mW)</th>
<th>Gain (dB)</th>
<th>$IIP_3$ (dBm)</th>
<th>Noise Figure (dB)</th>
<th>Area (mm$^2$)</th>
<th>Tech (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chih-Fan Liao (2007)</td>
<td>1.2-11.9GHz</td>
<td>1.8V</td>
<td>20mW</td>
<td>9.7</td>
<td>-6.2dBm</td>
<td>4.5-5.1dB</td>
<td>0.59mm$^2$</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Xiaohua Fan (2008)</td>
<td>2.2GHz</td>
<td>1.8V</td>
<td>9mW</td>
<td>20.4</td>
<td>-2.55dBm</td>
<td>1.92dB</td>
<td>-</td>
<td>0.35µm</td>
</tr>
<tr>
<td>Michael (2007)</td>
<td>3.1-10.6GHz</td>
<td>1.2V</td>
<td>9mW</td>
<td>15.1</td>
<td>&lt;4.3dBm</td>
<td>2.1dB</td>
<td>0.87mm$^2$</td>
<td>0.13µm</td>
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<tr>
<td>Donggu Im (2009)</td>
<td>50-880MHz</td>
<td>2.2V</td>
<td>34.8mW</td>
<td>14</td>
<td>3dBm</td>
<td>3dB</td>
<td>0.16mm$^2$</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Shana (2009)</td>
<td>2.4GHz</td>
<td>2.7V</td>
<td>81mW</td>
<td>32</td>
<td>-14dBm</td>
<td>3.2dB</td>
<td>2.54mm$^2$</td>
<td>0.5µm</td>
</tr>
<tr>
<td>Jonathan Borremans (2009)</td>
<td>5-6GHz</td>
<td>1.8V</td>
<td>6.5mW</td>
<td>14.8</td>
<td>-9dBm</td>
<td>2.6dB</td>
<td>0.14mm$^2$</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Chang (2006)</td>
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<td>1V</td>
<td>12.9mW</td>
<td>21.9</td>
<td>-11dBm</td>
<td>3.2dB</td>
<td>0.4mm$^2$</td>
<td>0.13µm</td>
</tr>
<tr>
<td>El Kaamouchi (2007)</td>
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<td>1.2V</td>
<td>6.5mW</td>
<td>13dB</td>
<td>--</td>
<td>3.6dB</td>
<td>0.5mm$^2$</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Ho and Mirabbasi (2007)</td>
<td>2.4GHz</td>
<td>1V</td>
<td>943μW</td>
<td>22.7</td>
<td>5.14dBm</td>
<td>2.8dB</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>Perumana (2005)</td>
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<td>1V</td>
<td>260 µW</td>
<td>13.6</td>
<td>7.2dBm</td>
<td>4.6dB</td>
<td>-</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Proposed Inductive Feedback CS LNA</td>
<td>2.4GHz</td>
<td>1.2V</td>
<td>32.26µW</td>
<td>20.34dB</td>
<td>-3.1dBm</td>
<td>3.90</td>
<td>0.1mm$^2$</td>
<td>120nm CMOS</td>
</tr>
<tr>
<td>Proposed Inductive Resistive Feedback CS LNA</td>
<td>2.4GHz</td>
<td>1.2V</td>
<td>2.88mW</td>
<td>18.79dB</td>
<td>-2.88dBm</td>
<td>3.45</td>
<td>0.11mm$^2$</td>
<td></td>
</tr>
<tr>
<td>Proposed Inductive Feedback CG LNA</td>
<td>0.342µW</td>
<td>21.28dB</td>
<td>-5.1dBm</td>
<td>4.51</td>
<td>0.1mm$^2$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed Inductive Resistive Feedback CG LNA</td>
<td>1.02mW</td>
<td>15.69dB</td>
<td>-</td>
<td>4.09</td>
<td>0.11mm$^2$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed Inductive Feedback Current reuse LNA</td>
<td>1.8µW</td>
<td>17.50 dB</td>
<td>-</td>
<td>1.55</td>
<td>0.13mm$^2$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
From the Table, it is seen that Common Gate inductive feedback LNA is the most suitable LNA for the design of low power transceivers intended for wireless sensor network applications. The power consumed in the proposed approach is less when compared to the other designs proposed in the literature.

3.3 MIXER

Mixer performs frequency translation by multiplying two signals. It has two input signals (RF signal and local oscillator signal) and the output is usually the product of these two inputs. The down conversion mixer transfers the spectrum from a high frequency band to a low frequency band.

Generally passive mixers have higher conversion losses and hence higher noise figures than the active mixers. They have higher linearity and speed. The active mixers have high conversion gain, low linearity with high power consumption. They are classified into single balanced mixers and double balanced mixers. Single balanced mixers are less complex, but have inferior performance in terms of RF to IF and LO to IF rejection, compared to double balanced mixers. Hence a double balance mixer is chosen here for the study.

3.3.1 Double balanced Gilbert cell Mixer

The most popular active, double balanced mixer topography in RFIC design is the Gilbert Cell mixer. This type of mixer exploits symmetry to remove the unwanted RF and LO output signals from the IF by cancellation. Since Gilbert mixers shown in Figure 3.54 are very much suitable for RF applications, it is used in the proposed transceiver design for down converting the RF signals into base band signals.
Figure 3.54 Gilbert cell using Double balanced Mixer

It works on the principle that a large local oscillator RF drive will cause switching/ modulating of the incoming radio frequency (RF) to low intermediate frequency (IF). The RF signal is applied to the transistors M2 and M3 which performs voltage to current conversion. Performance can be improved by adding inductive degeneration at the source terminals of M2 and M3. The MOS transistor M4 to M7 does the multiplication function. The mixer consumes a power of 1.44mW from the 1.2V supply at 2.4 GHz frequency using the 120 nm CMOS technology.

3.4 FREQUENCY SYNTHESIZER

The direct digital frequency synthesizer takes a large power consumption to synthesize very high frequencies directly. So a PLL based frequency synthesizer is used due to its high performance, namely low phase noise and low spurious tones. The performance evaluation of the PLL based frequency synthesizer in the transceiver is considered in this section.
3.4.1 PLL based Frequency Synthesizer

A typical PLL based frequency synthesizer presented by Lo and Luong (2002) is shown in Figure 3.55 which contains a reference source oscillating at frequency ‘f<sub>r</sub>’ and a VCO oscillating at frequency ‘f<sub>0</sub>’ . The two frequencies are compared in the phase detector. When the two phases are equal (phase locking), the output frequency is locked to the rational fraction of the reference frequency. The synthesizer is capable of generating a large number of highly accurate output frequencies.

![Schematic of PLL based Frequency synthesizer](image)

**Figure 3.55 Schematic of PLL based Frequency synthesizer**

3.4.2 Phase Detector and Loop Filter

The schematic uses an EXOR gate based phase detector. The purpose of the phase detector is to produce a signal that is proportional to the difference in phase between the two signals. Figure 3.56 explains how the variation in phase is detected using the EXOR based phase detector. The power consumed by the detector is only 14.438µW. When the PLL is in lock, this phase detector will generate a spur that is twice the frequency of ‘f<sub>r</sub>’. These spurs will be filtered by the loop filter. It is also used to stabilize the loop by introducing zeros and poles into the loop.
3.4.3 VCO and Frequency Divider

Figure 3.57 depicts the circuit of the typical Ring oscillator type voltage controlled oscillator. This configuration consumes a lower power of 0.322\(\mu\)W when compared to other circuits. The structure also employs positive feedback to achieve oscillation. The 1/2 frequency divider employs two latches in a master slave configuration with negative feedback.

Figure 3.57 Voltage Controlled Oscillator
3.5 BAND PASS FILTER

The third part of the receiver is band pass filter. Continuous-time filters, particularly $g_m$-C filters, are the most often used for signal frequencies of several Mega Hertz. The classical gyrator $g_m$-C topology reported by Thanachayanont (2002) is chosen for study. Figure 3.58 shows the single ended second order BPF topology. A Q-enhanced fully differential version of the circuit is considered here.

3.5.1 Second Order BPF Topology

The centre frequency is varied using the Equation (3.45) as,

$$\omega_0 = \sqrt{\frac{g_m g_m}{C_{gS} \left( C_{gS} + C_{m} \right)}}$$  \hspace{1cm} (3.45)

![Single ended second order BPF topology](image)

Figure 3.58 Single ended second order BPF topology

The Quality factor can be expressed by the Equation (3.46) as,

$$Q = \frac{\omega_0}{\left( \frac{g_{ds}}{C_{gS}} + \frac{g_m}{C_{gS} + C_{m}} \right)}$$  \hspace{1cm} (3.46)
The pass band gain is given by the Equation (3.47) as,

\[
K_0 = \left( \frac{g_{m_h} - C_{in}}{C_{g_{st}} \left( C_{g_{st}} + C_{in} \right)} \right) \left( \frac{g_{m_l}}{C_{g_{st}} + C_{in}} \right)
\]

(3.47)

Here, Q and \( K_0 \) are less than unity. So Q enhancement is necessary. The Q-factor and pass band gain can be improved by applying cascade and/or negative resistance cancellation techniques (Ismail 2000 and Thanachayanont 2001). In this topology in order to reduce the power consumed by the circuit the idle current sources are realized using current mirrors. By using this method the total current consumption of the circuit can be efficiently reduced without modifying its performance.

### 3.5.2 Q-Enhanced Classical Gyrator \( g_{m-C} \) Topology

![Figure 3.59 Basic Current mirror circuit](image)

The basic current mirror can be implemented using two MOSFET transistors as shown in Figure 3.59. The drain current of a MOSFET ‘\( I_D \)’ is a function of both the gate source voltage and the drain to gate voltage of the
MOSFET, which is given by \( I_D = f(V_{GS}, V_{DG}) \). For the transistor \( M_1 \), \( I_D = I_R \), since the reference current \( I_R \) is a known current which can be provided by a resistor \( R_1 \) to ensure that it is constant and independent of supply voltage variations.

With \( V_{DG}=0 \), the drain current of \( M_1 \) is \( f(V_{GS}, V_{DG}=0) \) such that \( f(V_{GS}, 0) = I_R \), which implicitly determines the value of \( V_{GS} \). Thus the current \( I_R \) sets the value of \( V_{GS} \). The circuit forces the same \( V_{GS} \) to apply to the transistor \( M_2 \). If \( M_2 \) also is biased with \( V_{DG}=0 \), then the transistors \( M_1 \) and \( M_2 \) have good matching of their properties such as channel length, width and threshold voltage. Then the relationship \( I_O = f(V_{GS}, V_{DG}=0) \) is applied by setting the current \( I_O = I_R \). Now the output current is same as the reference current when \( V_{DG}=0 \) for the output transistor, when both transistors are matched. The drain to source voltage can be expressed as \( V_{DS}=V_{DG}+V_{GS} \). With this substitution, the Shichman-Hodges model provides an approximate form for the function \( f(V_{GS}, V_{DG}) \),

\[
I_d = f(V_{GS}, V_{DG}) = \frac{1}{2} K_p \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})
\]

(3.48)

\[
= \frac{1}{2} K_p \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda (V_{DG} + V_{GS}))
\]

(3.49)

where, \( K_p \) is a technology-related constant associated with the transistor, \( W/L \) is the width to length ratio of the transistor, \( V_{GS} \) is the gate-source voltage, \( V_{th} \) is the threshold voltage, \( \lambda \) is the channel length modulation constant and \( V_{DS} \) is the drain source voltage.

Using the Equation (3.49), the power consumed by the transistor is determined as,

\[
P = V_{dd} \times I_d
\]

(3.50)
\[ I_0 = \frac{1}{2} K_p \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda (V_{DG} + V_{GS})) XVdd \]  

(3.51)

Figure 3.60 shows the Q-enhanced fully differential BPF using MOSFET current sources. There are four current sources in the circuit. Consider one of the current sources having the MOS transistors \( M_1 \) and \( M_2 \) and resistor \( R_2 \). If the transistors \( M_1 \) and \( M_2 \) are identical, then the drain currents are equal. Hence \( I_{D1} = I_{D2} \).

The drain current \( I_{D1} \) flowing through the transistor \( M_1 \) is represented by the Equation (3.52) as,

\[ I_{D1} = K_p (V_{GS1} - V_{th})^2 (1 + \lambda V_{DS1}) \]  

(3.52)

The drain current \( I_{D2} \) flowing through the transistor \( M_2 \) is represented as,

\[ I_{D2} = K_p (V_{GS2} - V_{th})^2 (1 + \lambda V_{DS2}) \]  

(3.53)

where, \( K_{p1} = K_{p2} = \frac{3W \tilde{\sigma}}{8L \tilde{\sigma}} K_x \)  

(3.54)

For the particular current source mentioned above, the output current \( I_0 = I_{D1} \) and the reference current \( I_R = I_{D2} \).

Using the Equations (3.52) and (3.53), the ratio \( \left( \frac{I_0}{I_R} \right) \) can be determined as,

\[ \frac{I_0}{I_R} = \left( \frac{W/L_1}{W/L_2} \right) \quad \text{(since } \lambda V_{DS} << 1 \text{).} \]  

(3.55)
From the Equation (3.55), it is observed that the output current is controlled by varying the values of (W/L) ratio. The gate length ‘L’ is fixed and the gate width ‘W’ is varied from device to device to give the desired current ratio (I_0/I_R). By choosing identical transistors, the current I_0 = I_R is obtained.

![Diagram of Q-Enhanced fully Differential BPF using four MOSFET current sources](image)

**Figure 3.60** Q-Enhanced fully Differential BPF using four MOSFET current sources

When compared to the circuit shown in Figure 3.58, the proposed circuit using MOSFET current sources consumes lower power of 123µW from the 1.2V supply.
3.5.3 Modified Q-Enhanced fully Differential BPF

In this topology, in order to further reduce the power consumed by the circuit, the resistors in the current mirrors are realized using active devices. In the MOSFET current source, since the transistors $M_1$ and $M_2$ are made identical, the output current $I_0$ exactly mirrors the current through the other transistor. Therefore this circuit can be used in our low power receiver design to filter out the unwanted frequency components. In this architecture, the resistances $R_1$, $R_2$, $R_3$ and $R_4$ are replaced by four MOSFETs $M_{17}$,$M_{18}$,$M_{19}$ and $M_{20}$. This modification is depicted in the Figure 3.61. The above modified circuit consumes a power of $50\mu W$ from the 1.2V supply. Table 3.10 shows the power consumption of the BPF architectures presented in this section.
### Table 3.10 Power Consumption of the BPF Architectures

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>BPF Schematics</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Second order Classical Gyrator $g_m$-C BPF Topology (Single ended)</td>
<td>1.21mW</td>
</tr>
<tr>
<td>2.</td>
<td>Q-enhanced fully differential BPF using MOS FET Current sources (Proposed Architecture)</td>
<td>123µW</td>
</tr>
<tr>
<td>3.</td>
<td>Modified Q-enhanced fully differential BPF (Proposed Architecture)</td>
<td>50µW</td>
</tr>
</tbody>
</table>

From the Table 3.10, it is observed that 89.83% of reduction in power consumption is obtained with Q-enhanced fully differential band pass filters using active current mirrors. Modified Q-enhanced fully differential BPF using all active devices are realized in the receiver design. In this case, 95.86% of reduction in power is obtained.

### 3.6 DETECTORS

Data demodulation is performed by the discrimination between presence (Data ‘1’) and absence (Data ‘0’) of signals.

#### 3.6.1 ASK Detector

For the demodulation of binary ASK, the coherent detector is used. The detector shown in Figure 3.62 consists of an integrator that performs a low pass filtering action and a decision device that compares the integrator output with a present threshold. The amplitude of the carrier signal is switched between either of the values corresponding to binary symbols ‘0’ and ‘1’.
3.6.2 FSK Detector

The FSK detector is shown in Figure 3.63. It consists of two correlators that are individually tuned to the two different carrier frequencies chosen to represent symbols 1 and 0. The decision device compares the output of the correlator with a preset threshold. If the threshold is exceeded, the detector decides in favour of symbol 1, otherwise it decides in favour of symbol 0.

3.6.3 PSK Detector

Figure 3.64 is a block diagram of a coherent detector for binary PSK signal detection. The received signal is integrated to perform the low pass filtering action. Then a decision device is used to compare the integrator output with a present threshold.
3.7 NOISE AND LINEARITY ANALYSIS OF THE RECEIVER

The noise figure of the two port network, based on available signal power can be calculated from the Equation (3.56) as,

\[ \frac{SNR_{in}}{SNR_{out}} = \frac{1}{G_{AV}} \left[ \frac{N_0}{G_{AV}KTB} \right] \]  \hspace{1cm} (3.56)

where, \( G_{AV} \) is the available power gain of the network, \( N_0 \) is the available noise power at the output of the network.

In 1944, Friis proved the noise figure for a cascaded system when the input and output of building blocks in the receiver were matched to a standard 50Ω / 70Ω impedance. As cited by Sheng Wenjum et al 2006, in a highly integrated receivers, the impedance of individual building blocks are usually unknown and different, and it is hard to apply power gain and NF concepts to base band blocks due to the high input impedance of the blocks. Hence using input-referred noise voltage and voltage gain to calculate NF of integrated receivers seems to be a better choice.

For the two port network, the total output noise can be referred back to input as a noise voltage source given by the Equation (3.57) as,

\[ \frac{V^2_{ni}}{V^2_{ni}} = \frac{V^2_{no}}{A^2_{ni}} \]  \hspace{1cm} (3.57)
The loaded voltage gain $A_{vn}$ is the gain at the load due to the actual input to the two port network given by the Equation (3.58) as,

$$A_{vn} = A_1 \frac{R_l}{(R_{out} + R_l)}$$  \hspace{1cm} (3.58)

In a cascade system, the cascaded-loaded voltage gain can be proved by the Equation (3.59) as,

$$A_{vn,Tot} = A_{vn,1} A_{vn,2} A_{vn,3}$$  \hspace{1cm} (3.59)

The cascaded NF can be calculated from the total noise voltage referred to the input of the system. The total receiver input referred noise voltage at LNA input would be referred by the Equation (3.60) as,

$$V_{ni,Tot}^2 = V_{ni,LNA}^2 + \frac{V_{ni,Mixer}^2}{A_{vn,LNA}^2} + \frac{V_{ni,Filter}^2}{A_{vn,LNA}^2 A_{vn,Mixer}^2}$$  \hspace{1cm} (3.60)

For a cascaded nonlinear system, the cascaded NF can be obtained from the Equation (3.61) as,

$$NF = 1 + \frac{V_{ni,LNA}^2}{A_{vn,LNA}^2} + \frac{V_{ni,Mixer}^2}{A_{vn,LNA}^2 A_{vn,Mixer}^2} + \frac{V_{ni,Filter}^2}{KTR_s}$$  \hspace{1cm} (3.61)

where,  
$T$ is the absolute temperature  
$K$ is the Boltzman constant  
$R_s$ is the source resistance

Assuming that the intermodulation products of each building block are all in-phase, which corresponds to the worst case scenario, the $IIP_3$ of the cascaded system can be proven by the Equation (3.62) to be (Razavi 1997),

$$IIP_3 = \frac{1}{KTR_s}$$  \hspace{1cm} (3.62)
\[
\frac{1}{V^2_{IP3i,Tot}} = \frac{1}{V^2_{IP3i,1}} + \frac{A^2_{sn,1}}{V^2_{IP3i,2}} + \frac{A^2_{sn,1}A^2_{sn,2}}{V^2_{IP3i,3}} \tag{3.62}
\]

### 3.7.1 Performance Comparison of ASK, FSK and PSK Receivers

Table 3.11 gives the comparison of the ASK, FSK and PSK receivers. The proposed receiver consists of a narrow band, inductive shunt feedback Common Gate LNA and a Gilbert cell for driving a second order all active resistor-less BPF and an ASK, FSK and PSK detector. All the circuits are either differential or pseudo differential. Self biased frequency synthesizer maintains 50 percent duty cycle which improves the LO edge transition.

**Table 3.11 Power summary of the ASK, FSK and PSK Receivers**

<table>
<thead>
<tr>
<th>Building Blocks</th>
<th>ASK Receiver</th>
<th>FSK Receiver</th>
<th>PSK Receiver</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG Differential LNA</td>
<td>0.659µW</td>
<td>0.659µW</td>
<td>0.659µW</td>
</tr>
<tr>
<td>Gilbert Mixer</td>
<td>1.44mW</td>
<td>1.44mW</td>
<td>1.44mW</td>
</tr>
<tr>
<td>BPF</td>
<td>50µW</td>
<td>50µW</td>
<td>50µW</td>
</tr>
<tr>
<td>Detector</td>
<td>0.68mW</td>
<td>0.9mW</td>
<td>0.68mW</td>
</tr>
<tr>
<td>Frequency Synthesizer</td>
<td>19.043µW</td>
<td>19.043µW</td>
<td>19.043µW</td>
</tr>
<tr>
<td><strong>Total Power Consumption</strong></td>
<td><strong>2.18mW</strong></td>
<td><strong>2.41mW</strong></td>
<td><strong>2.18mW</strong></td>
</tr>
</tbody>
</table>

In this work, the performance optimized common gate LNA is considered since it consumes a power of 0.659µW from the 1.2V supply at 2.4GHz radio frequency. It is considered as the analog front end for all the three types of receivers. Gilbert mixer consumes 1.44mW. Power consumption of the BPF is reduced by using active current mirror circuits. The conversion gain of the proposed ASK receiver is plotted in Figure 3.65 at various input frequencies.
Figure 3.65 Conversion gain versus input frequency of the ASK Receiver

Linearity is checked using two tones at 2.4GHz and 2.42GHz. The input referred third order intercept point $I_{IP3}$ found out from the Figure 3.66 is -19.1dBm. Similarly for the FSK and PSK transceivers $I_{IP3}$ is -12.45dBm and -14.57dBm respectively.

Figure 3.66 Input power versus Output power of the ASK Receiver

The simulated performance of the ASK, FSK and PSK receivers are tabulated in Table 3.12 for comparison.
Table 3.12 Performance Comparison of the proposed ASK, FSK and PSK Receivers

<table>
<thead>
<tr>
<th>Receiver</th>
<th>ASK</th>
<th>FSK</th>
<th>PSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$</td>
<td>&lt;-10dB</td>
<td>&lt;-10dB</td>
<td>&lt;-10dB</td>
</tr>
<tr>
<td>Rx conversion Gain</td>
<td>39.34dB</td>
<td>39.34dB</td>
<td>39.34dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>10.54dB</td>
<td>8.3dB</td>
<td>8.79dB</td>
</tr>
<tr>
<td>IIP$_3$</td>
<td>-19.1dBm</td>
<td>-12.45dBm</td>
<td>-14.57dBm</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-66.02dBm</td>
<td>-52.48dBm</td>
<td>-57dBm</td>
</tr>
<tr>
<td>Data Rate</td>
<td>840bps</td>
<td>750bps</td>
<td>20Kbps</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.18mW</td>
<td>2.41mW</td>
<td>2.18mW</td>
</tr>
</tbody>
</table>

The modified receiver design proposed in this research gives an improvement in performance when compared to the designs reported in the literature. It is tabulated in Table 3.13.

Table 3.13 Comparison of various Receivers and front ends in the literature

<table>
<thead>
<tr>
<th>References</th>
<th>Frequency (GHz)</th>
<th>Supply Voltage (V)</th>
<th>Power Consumption (mW)</th>
<th>Conversion Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>Technology (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Camus et al (2008)</td>
<td>2.4</td>
<td>1.35V</td>
<td>5.4mW</td>
<td>35dB</td>
<td>7.5dB</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Baoyong Chi et al (2007)</td>
<td>2.4</td>
<td>2.5V</td>
<td>15mW</td>
<td>&gt;11dB</td>
<td>&lt; 7.4dB</td>
<td>0.25µm</td>
</tr>
<tr>
<td>Zhan et al (2008)</td>
<td>2-5.8</td>
<td>1.4V</td>
<td>85mW</td>
<td>44dB</td>
<td>3.4dB</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Javinen et al (2005)</td>
<td>2.4</td>
<td>1.2V</td>
<td>3.3mW</td>
<td>47dB</td>
<td>28dB</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Lee et al (2007)</td>
<td>2.8</td>
<td>1.2V</td>
<td>51mW</td>
<td>23dB</td>
<td>4.5dB</td>
<td>65nm</td>
</tr>
<tr>
<td>Valla et al (2005)</td>
<td>5.5-8</td>
<td>1.2V</td>
<td>72mW</td>
<td>26dB</td>
<td>3.5dB</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Giuseppina Sapone et al (2008)</td>
<td>3-5</td>
<td>1.2V</td>
<td>10.8mW</td>
<td>23dB</td>
<td>3.4dB</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Wanghua Wu (2008)</td>
<td>17</td>
<td>2.5V</td>
<td>17.5mW</td>
<td>25-30dB</td>
<td>12 plus Mn 0.5dB</td>
<td>0.25µm BiCMOS</td>
</tr>
</tbody>
</table>
From the table, it is seen that the receiver designed by Javinen et al (2005) consumes a less power of 3.3mW when compared to the other receivers reported in the literature. They obtained the results at the expense of noise figure. In this research, the proposed ASK, FSK and PSK receivers are able to achieve moderate power consumption with good gain and improved noise figure, which is summarized in the above Table 3.12.