CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

In this work, a low power transceiver suitable for wireless sensor nodes is designed and implemented. The design efforts have been focused on the circuit level implementations. The critical benchmark for characterizing the performance of the transceiver is,

- Power consumption
- Noise figure
- Sensitivity
- Linearity
- Ease of input impedance matching relative to $50\Omega$ impedance
- Stability
- Data rate
- Output power

Several design proposals available in the literature are focused on the maximum output power, high data rate and good sensitivity of the transceiver. Power consumption is not concentrated much on these transceiver circuits.

Hence in this work, an effort was made to have low power transceivers without degrading the system performance. Circuits with lower power consumption sans degrading performance are desirable for extending the network life time of the sensor nodes and hence analytic expressions to
compute the parameters were derived to study the effect of the performance of the circuits used in the construction of the transceiver.

In order to design the low power circuits, several low power techniques such as sub threshold MOSFET operation, supply voltage scaling and reduction in parasitic capacitances are applied and tested on the transceiver circuits. With the advent of the rapid development of the CMOS technology, the proposed ASIC is simulated and implemented using 120nm standard CMOS process.

The design, theoretical analysis, simulations and implementations carried out for finding out the parameters of the proposed circuits have led to the following conclusions.

- Initially, the low power ASK, FSK and PSK modulators were designed and tested for their performance. It is found that,
  1. The total power consumed by the ASK modulator is only 200.104µW from the 1.2V supply at 2.4GHz frequency. It is less compared to the power consumption of the FSK (320µW) and PSK (5mW) modulators. Hence it is considered to design the low power transceiver for wireless sensor nodes.
  2. The PSK modulator is a power hungry modulator, it consumes 5mW of power. Even though it consumes more power its spectral efficiency is good. Hence it is suitable for high bandwidth WSN applications.

- Secondly, Power Amplifiers were taken for the study. It is seen that,
  1. To conserve battery power of the circuit, the power must be switched off whenever it is not in operation. This is
done by providing a power down switch using PMOS transistor controlled by an external control signal. With this power down switch, the power consumption of the designed power amplifier is reduced during sleep mode.

2. The power consumed by the non switching Class AB power amplifier with a power down switch is 192µW. compared to the other modified quasi complementary Class AB (200µW) and Class E (0.65mW) designs at 2.4GHz frequency from the 1.2V supply.

- Thirdly, LNAs were considered. The following five design proposals were made in this work.

(i) Inductive feedback Common Source LNA  
(ii) Series Inductive Resistive feedback CS LNA  
(iii) Inductive feedback Common Gate LNA  
(iv) Series Inductive Resistive feedback CG LNA  
(v) Current reuse Inductive feedback LNA

The power summary of the proposed LNAs is tabulated in Table 5.1.

**Table 5.1 Power summary of the proposed LNAs**

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Proposed LNA’s</th>
<th>Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Inductive Feedback CS LNA</td>
<td>32.26µW</td>
</tr>
<tr>
<td>2.</td>
<td>Inductive Resistive Feedback CS LNA</td>
<td>2.88mW</td>
</tr>
<tr>
<td>3.</td>
<td>Inductive Feedback CG LNA</td>
<td>0.342µW</td>
</tr>
<tr>
<td>4.</td>
<td>Inductive Resistive Feedback CG LNA</td>
<td>1.02mW</td>
</tr>
<tr>
<td>5.</td>
<td>Inductive Feedback Current reuse LNA</td>
<td>1.8µW</td>
</tr>
</tbody>
</table>
From the design and analysis it is clear that,

1. The power consumed by the single ended inductive feedback common gate LNA is only 0.346μW from the 1.2V supply at 2.4GHz frequency at the expense of the noise figure of 4.51dB. The gain of the CG LNA is 21.28dB which is obtained by boosting the transconductance ‘$g_m$’ of the transistor.

2. Current reuse LNA gives astonishingly less noise figure of 1.55dB. Also it consumes a power of 1.25μW at the 2.4GHz frequency.

3. A comparison of the performance of the proposed design with the existing results in the literature shows that the proposed LNAs give better performance in terms of noise figure, gain and the power consumption. The LNAs also give acceptable impedance matching and linearity over a range of frequencies.

4. As the supply voltage increases, gain improves considerably. Also it is observed that the power consumption of the LNA reduces with the reduction in supply voltage.

- Fourthly, Band pass filters were taken into consideration. From the modified design and analysis it is observed that,

1. Constant current sources are replaced with active current mirror circuits in order to reduce the power consumption of the BPF. From the simulations and analysis it is seen that 89.83% reduction in power is obtained using this technique.
2. Resistive loads are replaced in the modified BPF circuit using active devices in order to consume less power and to reduce the area occupied by the integrated circuits. Still a reduction in power of 95.86% is observed in this case.

Finally, ASK, FSK and PSK transceivers were designed using the proposed wireless components and implemented. From the design proposals, it is found that,

1. The proposed transceivers use direct digital modulation transmitter and low IF receiver architecture, consisting of inductive shunt feedback Common Gate LNA and a Gilbert cell mixer for driving a second order all active resistor less Band pass filter and a Detector.

2. The ASK transceiver consumes 0.41mW during transmission and 2.18mW during reception. The FSK and PSK transceivers consume 0.53mW and 5.21mW in the transmit mode and 2.41mW, 2.18mW in the receive mode respectively. Hence, in this research, the ASK transceiver is considered for the low power WSN since it consumes less power when compared to the FSK and PSK Transceivers.

3. The PSK transceivers are suitable for high bandwidth and high data rate applications, since it can transmit signals at a data rate of 20Kbps. It is quite higher when compared to the data rate obtained by the ASK (840bps) and FSK (750bps) transceivers.
4. The circuits are implemented using 120nm CMOS process technology. From the Layout, it is seen that the area occupied by the transceiver circuits are less than the area occupied by the transceiver circuits available in the literature.

5. The Layout of the ASK transceiver consumes less area of 0.5 mm$^2$ using the 120nm CMOS technology. It is less compared to the area occupied by the FSK (0.52 mm$^2$) and PSK (0.55 mm$^2$) transceivers.

6. Frequent topology changes do not arise since the nodes are operated for longer duration. Also the link failure is less and the cost of redeployment phase is minimum. It ensures the reliable operation.

7. Thus the low power Transceiver is designed for low power wireless sensor nodes.

5.2 SCOPE FOR FUTURE WORK

There are a few considerations that can be explored further. For Wireless sensor nodes, in order to accommodate large amount of circuitry in a small chip the dimension of the devices should be made smaller. The performance of the transceiver is expected to improve when the device magnitude scales down. The transceivers can also be implemented using the advanced CMOS technologies at the expense of short channel effects such as velocity saturation, mobility degradation and drain-induced barrier-lowering. The shorter the channel length, the more severe these effects are. Some work has already begun in this area, and it offers a wide open scope for future innovations.