ABSTRACT

Conventional non-adaptive filters perform well as long as the input signal is varying uniformly with noise. Reconfigurable computing has been proposed for signal processing applications with various objectives, including high performance, flexibility, specialization and most recently, adaptability. A reconfigurable processor can be viewed as taking its inspiration from the paging mechanism in operating systems with the concept extended to hardware logic circuits. However, there are some important distinctions when extending the paging concept to hardware. In the paging concept the code being swapped between RAM and disk usually represents a single thread of control, whereas, in the hardware context, the logic can be concurrent. Reconfiguration is characterized by how fast the reconfiguration can occur and how many possible reconfigurations can be used (dynamic reconfiguration). A dynamically reconfigurable system allows the various components of the processor to update and even completely change the functions implemented in the programmable device without the need for a system reset or power down. Also, partial reconfiguration can occur without affecting the continuity of the device operation.

For many signal processing systems, it is possible to exploit certain signal characteristics to optimize computation and memory requirements. In this work, an FIR filter based on reconfigurable fabric is proposed for an adaptive noise cancellation application. The filter is designed to reconfigure
itself and provide real-time noise cancellation. The filter logic is implemented on a novel reconfigurable fabric designed for the specific purpose of implementing an FIR filter using primitive operators and is synthesized on a Xilinx FPGA hardware chip. The work is the first operational implementation of the reconfigurable architecture and its algorithm and is targeted to the Virtex-II FPGA hardware to take advantage of computational specialization and parallelism. The work has the capability to adaptively alter the amount of computation performed and the amount of storage used, at both fine-timescale and coarse-timescale level. An important objective index that reflects the physiological activity of fetus heart electricity, namely the fetal heart rate, is extracted in this work. The algorithms presented have quick convergence time. The comparison studies done in this work will assist in estimating the VRCs influence in the integration of Field Programmable Gate Array (FPGA) based evolvable systems and provide high performance benefits. The work provides a scope for implementation of new standards and protocols on an as-needed basis by protecting the investment in computing hardware. It functions as a programmable hardware with higher performance, flexibility of a software based solution, while retaining the execution speed of a more traditional hardware based approach.