A Biological Neural Network (BNN) forms the Central Nervous System, which has highly interconnected neurons to co-ordinate all the functions like reading and thinking. ‘Artificial Neurons’ are simple abstractions of biological neurons, programmed in software or modeled in hardware. Networks of artificial neurons known as Artificial Neural Networks (ANN) have a fraction of power of biological neural structures, and they can be trained to solve many complex problems. An ANN has the ability to learn, and it had been realized in software. But, learning is a recursive process involving multiple iterations which takes a long time, when implemented in software. However, availability of powerful resources at affordable cost has opened up the interesting possibility of realizing ANN in hardware. The focus of the present work is on Very Large Scale Integration (VLSI) hardware realization of ANN so as to achieve flexibility, portability and adaptability.

The approach for hardware implementation of ANN can be digital, analog, mixed-signal or pulse-stream based designs. Out of these, purely analog design - being non programmable - is not pursued further in the present work. Rather, an efficient hybrid approach that combines ANN and Genetic Algorithm (GA), bringing up the Genetically Evolved Neural Network (GENN) is explored in the digital domain. Digital architectures exhibit simplicity, flexibility, maturity and adaptability. In order to facilitate re-programmability, weights of the compact analog architectures are learnt.
and stored digitally. Thus the mixed-signal architectures are explored. Another form of mixed-signal design namely, Pulse Density Modulation (PDM) based architecture is extensively studied. It helps to utilize the advantages of digital designs by representing signals in pulses. So far, gradient-based techniques have been adopted, to design the architectures of ANN. They are good at fine-tuning but the objective function is decreased locally, without considering the entire search space. When the network is trained by conventional dynamic construction method to satisfy the learning precision, another optimization technique like GA is to be used to prune the network.

The implementation is executed in four phases of two different architectures each. The first digital architecture developed, the Medical Expert System (MES) that diagnoses the bladder and breast cancer. The second architecture utilized layer-multiplexing concept, which realizes only the largest layer in hardware. The same layer is pruned to realize the rest of the layers sequentially. The second phase of work, implements the ANN in mixed-signal design domain. Instead of using any conventional SPICE tools, the Simulink tool is used to model the MOSFETs and hence the neuron and the network. It sheds light, in the direction of hardware/software co-design. The architecture solves the Parity-N problem with N/2 hidden layer neurons, which is otherwise reported to be N neurons. The first PDM architecture of third phase has piecewise linear activation function and the second architecture has on-chip simultaneous perturbation learning. The final phase explains the development of the Genetically Evolved Neural Network
(GENN). The genetic evolution of Feed-Forward Neural Network (FFNN) to solve N-bit parity problem has resulted in the architecture with N/2 neurons in the hidden layer.

Digital architectures allow the designer to reconfigure the hardware. The layer-multiplexing scheme conserves area, which facilitates a portable environment. Analog modules of mixed-signal approach, offer compact designs that improve speed. On the other hand, the pulse-stream representations in digital domain offer robustness and re-programmability. Finally, the genetic evolution optimizes area by reducing the number of neurons and hence speeds up the process. Thus the objectives are met through the execution of four different phases of design.

Synthesized results of PDM architectures solving XOR and parity functions exhibit compactness by consuming, only around 5% and 16% of logic cells. The design includes learning module on-chip, which needs mentioning. It is observed from the genetically evolved ANN that the synthesis of XOR and 8-bit parity function has consumed around 17% and 42% of silicon resources in terms of slices. It ensures that high capacity Virtex target device can ease the implementations of complex architectures.