# CHAPTER 5
## DESIGN AND DEVELOPMENT OF THE HARDWARE

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CHAPTER 5
DESIGN AND DEVELOPMENT OF THE HARDWARE

5.1 Introduction

In this chapter the design and development of digital controller for the induction motor using dsPIC30F2010 controller has been discussed, which includes overview of dsPIC30F2010, design of power circuit and control circuit. The over view of dsPIC30F2010 includes the details of controller features and advantages. The power circuit design deals with the design of three phase rectifier, inverter and regulated power supply. The design of controller circuit is done using dsPIC30F2010 controller and it deals with isolation and driver circuit with the help of TLP 250, speed sensing circuit have been discussed in this. The rating of induction motor used for the design and development of hardware are as given below:

- Voltage rating : 415V
- Current rating (full load) : 1.8A
- Power rating : 1 HP (746 watts)
- Stator and rotor resistance per phase : 10.05Ω
- Efficiency : 75.5%

5.2 Overview of dsPIC30F2010

The dsPIC30F2010 is a single chip high performance 16-bit digital signal controller (DSC), which has the “heart” of a 16-bit microcontroller unit (MCU) with robust peripherals and fast interrupt handling capability and the “brain” of a digital signal processor (DSP) that manages high computation activities, creating the optimum single-chip solution for embedded system designs.

The dsPIC DSC can be used for real time systems applications because of its superior performance over 16 and 32 bit microcontrollers. It has also a number of highly
enabling features specifically designed to enhance system reliability and reduce system cost by eliminating external components. Table 5.1 shows the Motor Control and Power Conversion Family features.

**Table 5.1 dsPIC30F2010 Motor Control and Power Conversion Family**

<table>
<thead>
<tr>
<th>Device</th>
<th>Pins</th>
<th>Program Mem./Bytes/Instructions</th>
<th>SRAM Bytes</th>
<th>EEPROM Bytes</th>
<th>Timer/16-bit</th>
<th>Input Cap</th>
<th>Output Comp./Std PWM</th>
<th>Motor Control PWM</th>
<th>A/D 10-bit 1 Mmps</th>
<th>QEI</th>
<th>UART</th>
<th>SPI</th>
<th>i²C/TM</th>
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<tr>
<td>dsPIC30F2010</td>
<td>28</td>
<td>12K/4K</td>
<td>512</td>
<td>1024</td>
<td>3</td>
<td>2</td>
<td>6 ch</td>
<td>6 ch</td>
<td>Yes</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Some of the special hardware features as compared to other controller is as given below:

- It has reliable watch dog timer, which can be enabled by flash configuration bits and selecting its period. This can be achieved from its internal oscillator without disable of system clock.
- It has on-chip system clock monitor which can monitor and detect the system clock failures in turn it forces to reset the chip.
- These dsPIC30F devices operate up to maximum of 125°C temperature. Hence, it can be used for motor control, power conversion and lighting control etc.
- Using this device, it is possible to drive LED’s directly without external FET switches because of input / output in sources or sinks at 25 milliamps, which inturn it reduces the cost and space.
- It has the Harvard Architecture.
- It has two internal timers namely: Programmable power up timer (PWRT) and oscillator start up timer (OST). The PWRT provides a delay on power up only, which
keeps the port in reset while the power supply stabilizes. The OST keeps the chip in
reset mode until the crystal oscillator is stable.

- It has three primary clock oscillators: XTL, XT and HS. The XTL oscillator is
designed for crystals or ceramic resonators in the range of 200 KHz to 4 MHz. The
XT oscillator is designed for crystals and ceramic resonators in the range of 4 to 10
MHz. The HS oscillator is for crystals in the 10 to 25 MHz range. These oscillators
are available at OSC1 and OSC2 pins.

5.2.1 The prominent features of dsPIC30F2010

Fig.5.1 shows the block diagram of dsPIC30F2010 and it has following prominent
features.

High-Performance Modified RISC CPU:

- Modified Harvard architecture
- 24-bit wide instructions, 16-bit wide data path
- 12 Kbytes on-chip Flash program space
- 512 bytes on-chip data RAM
- 1 Kbyte non-volatile data EEPROM
- 16 x 16-bit working register array
- Up to 30 MIPS operation
- 27 interrupt sources
- Three external interrupt sources
- Eight user-selectable priority levels for each interrupt
Fig. 5.1 Block diagram of dsPIC30F2010

**DSP Engine Features:**

- Modulo and Bit-Reversed modes
- Two 40-bit wide accumulator
- 17-bit x 17-bit single-cycle hardware fractional/ Integer multiplier
- Single-cycle Multiply-Accumulate (MAC) Operation
- 40-stage Barrel Shifter
- Dual data fetch

**Peripheral Features:**

- High current sink/source I/O pins: 25 mA/25 mA
- Three 16-bit timers/counters; optionally pair up 16-bit timers into 32-bit timer modules
- Four 16-bit capture input functions
- 3-wire SPI modules (supports 4 Frame modes)
- I²CTM module supports Multi-Master/Slave mode
• Addressable UART modules with FIFO buffers

**Motor Control PWM Module Features:**
• Six PWM output channels
• Four duty cycle generators
• Dedicated time base with four modes
• Dead-time control for Complementary mode
• Manual output control

**Analog Features:**
• 10-bit Analog-to-Digital Converter (ADC) with:
  • Six input channels
  • Conversion available during Sleep and Idle.

### 5.2.2 Architecture of dsPIC30F2010

The architecture of dsPIC30F2010 is as shown in Fig 5.2. The core has a 24-bit instruction word. The Program Counter (PC) is 23 bits wide with the Least Significant bit (LSB) always clear and the Most Significant bit (MSB) is ignored during normal program execution, except for certain specialized instructions. Thus, the PC can address up to 4M instruction words of user program space. An instruction pre-fetch mechanism is used to help maintain throughput.

Program loop constructs, free from loop count management overhead, are supported using the DO and REPEAT instructions, both of which are interruptible at any point. The working register array consists of 16x16-bit registers, each of which can act as data, address or offset registers. One working register operates as a software stack pointer for interrupts and calls. The data space is 64 Kbytes (32K words) and is split into two blocks, referred to as X and Y data memory. Each block has its own independent Address Generation Unit (AGU). Most instructions operate only through the X memory AGU, which provides the appearance
of a single unified data space. The Multiply-Accumulate (MAC) class of dual source DSP instructions operate through both the X and Y AGUs, splitting the data address space into two parts. The X and Y data space boundary is device specific and cannot be changed by the user. Each data word consists of 2 bytes, and most instructions can address data either as words or bytes.

There are two methods of accessing data stored in program memory:

• The upper 32 Kbytes of data space memory can be mapped into the lower half (user space) of program space at any 16K program word boundary, defined by the 8-bit Program Space Visibility Page (PSVPAG) register. This uses any instruction access program space as if it were data space, with a limitation that the access requires an additional cycle. Moreover, only the lower 16 bits of each instruction word can be accessed using this method.

• Linear indirect access of 32K word pages within program space is also possible using any working register, via table read and writes instructions. Table read and write instructions can be used to access all 24 bits of an instruction word. Overhead-free circular buffers (modulo addressing) are supported in both X and Y addresses spaces. This is primarily intended to remove the loop overhead for DSP algorithms.

The X AGU also supports bit-reversed addressing on destination effective addresses, to greatly simplify input or output data reordering for radix-2 FFT algorithms. The core supports Inherent (no operand), Relative, Literal, Memory Direct, Register Direct, Register Indirect, Register Offset and Literal Offset Addressing modes. Instructions are associated with predefined Addressing modes, depending upon their functional requirements. For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, 3-operand instructions are supported, allowing C = A+B
operations to be executed in a single cycle. A DSP engine has been included to significantly enhance the core arithmetic capability and throughput. It features a high speed 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bi-directional barrel shifter. Data in the accumulator or any working register can be shifted up to 15 bits right or 16 bits left in a single cycle.

A DSP engine has been included to significantly enhance the core arithmetic capability and throughput. It features a high speed 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bi-directional barrel shifter. Data in the accumulator or any working register can be shifted up to 15 bits right or 16 bits left in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC class of instructions can concurrently fetch two data operands from memory, while multiplying two W registers. To enable this concurrent fetching of data operands, the data space has been split for these instructions and linear for all others. This has been achieved in a transparent and flexible manner, by dedicating certain working registers to each address space for the MAC class of instructions. The core does not support a multi-stage instruction pipeline. However, a single stage instruction pre-fetch mechanism is used, which accesses and partially decodes instructions a cycle ahead of execution, in order to maximize available execution time. Most instructions execute in a single cycle, with certain exceptions. The core features a vectored exception processing structure for traps and interrupts, with 62 independent vectors. The exceptions consist of up to 8 traps (of which 4 are reserved) and 54 interrupt. Each interrupt is prioritized based on a user assigned priority between 1 and 7 (1 being the lowest priority and 7 being the highest) in conjunction with a predetermined ‘natural order’. Traps have fixed priorities, ranging from 8 to 15.
Fig. 5.2 Architecture of dsPIC30F2010
5.2.3 Advantages of Digital Signal Controller over Microcontroller Unit and Digital Signal Processing

It has both MCU and DSP characteristics. The main advantage of dsPIC is that it posse’s merits of both MC and DSP. The cost of dsPIC is comparatively lower than that of DSP. The arrangement is very simple and thus reduces complexity. It has high efficiency. Programming is handy as the C language is used to write the program.

5.2.4 Software development tools

There are large number of software and hardware development tools integrated within one software package called MPLAB Integrated Development Environment (IDE). MPLAB IDE is a software program that runs on a PC to develop applications for microcontrollers. It is called an IDE because it provides a single integrated environment to develop code for embedded microcontrollers. It has both built-in components and plug-in modules to configure the system for a variety of software and hardware tools. Built into IDE are program editor, project manager, powerful debug tools, assembler/linker, language tools and execution engines.

Program editor has been used to write source code and save it as a file. Source code is written for the built-in assembler and compiler. A text editor was used to write the code specially designed for writing code for microcontrollers. It recognizes C programming syntax and automatically uses different colours to identify comments, labels, and reserved words to help programmer quickly spot syntax errors. After the code is written, the editor work with the other tools to display code execution in the debugger.

Project manager allows different source files to be grouped and then sent to the select set of software tools such as assembler, compilers, librarians and linkers to build the final application. The assembler can be used to assemble a single file or can be used with the linker to build a project from separate source files, libraries and recompiled objects. The
linker is responsible for positioning the compiled code into memory areas of target microcontroller. It takes care of assigning register location of variables, and ensuring that each source modules can access function and variables from other source modules. When using language tools for embedded systems, a “cross-assembler” or “cross-compiler” is used. These tools differ typical compilers since they run on a PC but produce code to run on another microprocessor, hence they “cross-compile” code for a microcontroller that uses an entirely different set of instructions from the PC. The language tools also produce a debug file that IDE uses to correlate the machine instructions and memory locations with the source code. Execution engines such as software simulators in IDE for all Microcontrollers use the PC to simulate the instructions and peripheral functions of the microcontroller devices.

5.3 Design of three phase full bridge rectifier

In this section, the design of three phase full wave bridge rectifier has been discussed. The design has been carried out using twelve power diodes (D1 – D12), filter capacitors (C1 & C2), three safety fuses (F1-F3) and three metal oxide varistors (M1-M3) as shown in Fig 5.3 and its detailed discussion is given below.

Selection of power diodes:

The power diodes used in this work are 6A10BL, which has the rating of 6 Amps and 1000 volts. These diodes are able to handle the peak voltage in reverse direction (PIV). These diodes block the reverse voltage of approximately 6000 volts (without any spike in the input voltage). It also conducts the full load current at 1.8 Amps during forward bias effectively.
Fig. 5.3 Three phase full bridge rectifier

The rating of the power diode (6A10BL) is as given below:

- Maximum recurrent peak reverse voltage : 1000 V
- Maximum RMS voltage : 0700 V
- Maximum DC blocking voltage : 1000 V
- Max. Average forward rectified current : 6A

In this work, the three phase bridge rectifier has been designed using three legs. Each leg has two diode sets namely upper and lower sets. Each set has two diodes connected in parallel to increase the current rating of 12 amps, which is sufficient to handle a 1.8 amps, 415V and 1HP motor.

We have

\[
PIV = \sqrt{3} \times V_{mp} \hspace{1cm} (5.1)
\]

But \( V_{mp} = \sqrt{2} \times V_{phase} \) \hspace{1cm} (5.2)
Therefore, \[ V_{\text{phase}} = \frac{415}{\sqrt{3}} \]
\[ V_{\text{phase}} = 239.6003 \text{V} \]
\[ V_{mp} = 338.8 \text{V} \]

and \[ PIV = 586.89 \text{V} \]

The selected device is more than five times the rating of motor.

**Selection of Filter capacitors:**

The output of the bridge rectifier contains ripples. In order to reduce the ripples the C-type capacitor has been used and it also withstands the average of DC link voltage. In order to achieve these, following steps are used to determine the capacitor value.

\[
V_{av} = \frac{3\sqrt{2} \times V_{L-L}}{\pi} \quad \text{------------------ (5.3)}
\]
\[
= 1.35 \times 415 \quad \text{------------------ (5.3)}
\]
\[
= 560.25 \text{ V}
\]

To withstand this voltage, two capacitors of voltage rating 450V each are connected in series, making the total withstanding capability as 900V.

We know that

\[
C = \frac{1}{4fR} \left[1 + \frac{1}{\sqrt{2fRF}}\right] \quad \text{------------------ (5.4)}
\]

Where effective load resistance \( R \) is given by

\[
R = \frac{V_{av}}{I_0} = \frac{560.25}{1.8} = 311.25
\]

\[
% \text{Ripple} = 1 \quad \text{and} \quad f = 50 \text{Hz},
\]

by Substitute the values of \( R \), \( RF \) and \( f \) in equation 5.4, we get as, \( C = 27\mu \text{F} \).
In order to increase the withstand voltage, two capacitors of voltage rating 450V and 27µF each are connected in series, making the total withstanding capability as 900V.

**Selection of safety Fuses:**

To protect the rectifier circuit from short circuit, three fuses F1, F2 and F3 are used and are connected in the line input as shown in the Fig 5.3. They are used to protect against the starting current which is order of 1.8 amps.

**Selection of Metal Oxide Varistors (MOVs)**

During switch action of the input supply, voltage surges may damage the power diodes and the inverter-motor system. In order to protect the circuit from the transient voltage, the Metal Oxide Varistors (M1, M2 and M3) are used. Three MOV’s are connected between any two input lines as shown in Fig 5.3. Since peak value of input line to line voltage is 587 V, we have to choose the device having the rating above this voltage so that any voltage spike above this range is suppressed. Hence, MOV TVR 14621 is used in the present design. It is capable of suppressing the voltage spikes of 2500V.

**5.4 Design of Three Phase full-bridge IGBT based Inverter**

The design of three phase full wave bridge inverter using IGBT has been discussed in this section. The components used for the design of inverter circuit is as follows.

The components used for the design of inverter circuit are as follows:

- IGBTs (Q1 to Q6)
- Power diodes (D1 to D6)
- Snubber circuits
  - Capacitor (C1 to C6)
  - Resistance (R1 to R6)
Fig. 5.4 Three phase full bridge inverter
Selection of power IGBTs:

The selection of IGBT was done on the basis of voltage, current and power rating of the induction motor. Also the maximum reverse voltages available across its collector and emitter terminals are taken into consideration.

The maximum reverse voltage, which is same as dc link voltage is given by equation (5.3):

\[ V_m = \frac{3\sqrt{2} \times V_{l-1}}{\pi} \]

\[ = 1.35 \times 415 \]

\[ = 560.25 \text{ V.} \]

In order to meet the requirements, the Fairchild’s FGA25N120ANTD –IGBT have been selected and the current and voltage rating is given below:

- Voltage rating : 1200V
- Current rating : 25 A

Design of Snubber circuit:

The semiconductor switching devices are having some disadvantages such as rapid change in voltage causes the device to trigger spuriously or turn on partially. This malfunction may cause the damage of control circuit switches or load. In order to overcome these drawbacks a snubber circuit is used. In this present work, RC type snubber circuit is used and its design is as given below:

Selection of capacitor:

The selection of Snubber capacitors are based on peak voltage, rms current and rate of change of voltage. The criterion for selection of capacitor is given by the following relation:

\[ C_s = \frac{I_{0t_s}}{2V_o} \]

---------------------------------- (5.5)
Where $I_0$ is the average load current, $t_s$ is the fall time of the switch current and $V_o$ is the dc voltage across the inverter.

For fall time = 180nsec, $I_0 = 1.8$Amps and $V_o = 560.25$V and substituting these values in the equation (5.5), the approximate value of capacitor obtained is $C_s = 0.2 \text{ nF}$

**Selection of Resistance:**

The resistance is selected on the basis of following formula:

$$T_{\text{on state}} > 2.3 R_s C_s$$

Hence the value of resistance is chosen as 200 ohm.

**5.5 Design of DC Regulated Power Supply**

In the proposed system 15 V, 12 V and 5 V DC power supply are required for controller, firing circuit and driver circuits. The required power supply was obtained by the designed circuits as shown in Fig 5.5 and Fig 5.6 respectively. The 5V DC regulated power supply was obtained from the 230V, 50Hz AC supply using step down transformer of 230V/5-0-5V. The output of transformer is 5V AC. This ac voltage was converted into 5V DC using rectifier circuit consisting of 4 diodes (IN4007). The output of rectifier consists of ripple. In order to remove the ripple a filter circuit is used. The output of filter gives the pulsating DC power.

For all IGBT’s driver power supplies, six step down transformers of voltage ratio 230/12-0-12 and two step-down transformer of voltage ratio 230/15-0-15 are used for Digital signal controller and isolation circuit.

Four +12V supply are required for firing gates of six IGBTs. Three separate +12V supply for upper switches and one common for all lower switches because their sources (negative of each gate) are shorted/common as shown in Fig. 5.6.
Single phase 230V, 50Hz supply is given to the step-down transformer, and then it is rectified using diode rectifier. Here IN4007 diodes are used. The rectified output contains ripples, so to eliminate these ripples capacitors of value 1000 microfarad at rectifier output and 100 microfarad at voltage regulator output are used as shown in Fig.5.8. The output of the rectifier is given to a voltage regulator to regulate/sustain the DC voltage. For +12V/+15V DC voltages LM7815/LM7812 voltage regulators are used.

Fig 5.5  +5V DC regulated power supply
Fig 5.6 +12V DC regulated power supply
5.6 Design of control circuit

In this section, the detail discussion of design of control circuit is presented. The control circuit has two sections, namely Digital signal controller section and isolation and gate driver circuit section. The details of each section is discussed as follows

5.6.1 Digital Signal Controller Circuit Part

The control circuit of the proposed scheme consists of a dsPIC30F2010 Digital Signal Controller and a gate driver circuit for the generation of pulses of required frequency. The controller has operated at 25MHz crystal frequency. The internal timer is used for clock generation and a counter is used for counting the pulses from the proximity sensor. According to the requirement, a software program is written and is fed to the controller, which decides the frequency of pulse to be applied to the gate of the IGBTs. The control software essentially compares the set speed (reference speed) and the actual speed (feedback speed) of the motor. Based on the difference between these two speeds, it decides the control scheme; whether to increase/decrease the pulse frequency or to keep it constant i.e. the difference in speed is used to adjust the frequency of the firing pulse given to the gate of IGBTs in order to bring the motor speed to the desired or set speed. The controller also decides the instant timing of the gate signal to be given to the IGBTs, in order to avoid the overlapping in conduction of incoming and outgoing IGBTs. Because the overlapping in conduction leads to the short circuiting of dc supply, which causes the damage to IGBT’s.

The design of control circuit has been carried out using dsPIC30F2010 digital signal controller (DSC), which has the features of both microcontroller as well as digital signal controller. This controller is used in this work because of its advantages such as fast interrupt handling capability, reduces the complexity of control circuit, faster in computation, smaller in size, lesser in cost and increases in overall efficiency.
The connection diagram of the controller is as shown in Fig.5.7. It has on-chip oscillator and clock circuitry, which requires an externally connected crystal.

- Port E is used for PWM channels. Pin no. 21 to 26 are utilized for driving the gate triggered circuit. Each pin is responsible for its corresponding Gate i.e. G1, G2, G3, G4, G5 and G6.
- 25 MHz crystal is connected between pin no. 9 and 10.
- Pin no. 2, 3, 4, 5, 6, 7, 12 are utilized for the LCD display. The program is written for displaying the reference speed and present speed of the motor. An ADC channel is used to input the speed command.
- Pin no 1 is used to reset the IC.
- Pin 16 and 17 are connected to speed changing switches.
- Pin no 11 is used for RPM feedback.
- Pin no 27 is used as ground for Analog module.
- Pin no 28 is used as supply for Analog module.
Fig 5.7 Connection diagram of digital signal controller.

**System Design:**

The designed controller carries out the following sequence of operations:

- Receives input from sensors and samples the measured value.
- Compares this measured value with the set value and establish the error.
• Makes the calculations based on error value and stores the values of previous inputs and outputs to obtain output signal.

• Sends the output signal to PWM generators.

• Waits until the next sample time before repeating cycle.

![Block Diagram of Controller]

**Fig. 5.8. Internal block diagram of Controller**

### 5.6.2 Isolation and gate driver circuit

The driver circuit operates at very low power levels. The driver circuits are connected to power devices which operate at high power levels. If the power device is damaged, then high voltage will get connected to drive circuit, this will damage the drive circuit also, so there must be some electric isolation between control and power circuit.

Fig. 5.9 shows the isolation and gate driver circuit. The main functions of isolation and gate drive circuit are:

• To provide required gate voltage and current to IGBTs for switching.

• To transmit the control signals to the bridge circuit faithfully.

• Provides electrical isolation between power switch and control circuit.
• Driver circuit amplifies control signals to required level for switching of power switch.

In the proposed scheme there are six IGBTs in the three phase bridge inverter. So separate isolator and driver circuits are used to drive each of IGBT’s. The pulses available at the output of the logic circuit are given to the six individual gates. Only one is shown in the figure, others are identical in nature.

![Isolation and gate drive circuit](image)

**Fig.5.9 Isolation and gate drive circuit**

The dc supply required for driver circuit is derived from the dc regulated power supply section. The supply is given to the optocoupler TLP250 as shown in Fig 5.9. The control circuit generates the required gate pulses of the specified voltage called gate voltage and it is applied between the gate and emitter terminal of the IGBT. There is a need of isolation and interfacing circuit between the IGBT and control circuit. This is achieved by using optocouplers and pulse transformers.

The optocoupler consists of an ILED and a phototransistor. When the signal is applied to the ILED, then it turns on and it emits light. When emitted light falls on optocoupler then the photo transistor starts conducting. Each drive circuit consists of one optocoupler, totem pole arrangement of npn and pnp transistors (Q2 and Q3) and one BC547 npn transistor (Q1)
to drive the totem pole stack. Resistor R1 limits the current through light emitting diode of integrated circuit TLP250. Resistance R1 acts as drive resistance for LED and R4 is designed to sweep out the stored charges at the transistor region.

The current through the collector of conducting transistor Q1 is given by:

$$I_c = \frac{V_{\text{supply}} - V_{\text{CEsat}}}{R_c + 100\Omega + 100K\Omega}$$

Where, \(R_c\) (Collector resistance) = 1K\(\Omega\)

and, \(V_{\text{CEsat}} = 0.3V\)

Therefore, the collector current becomes

$$I_c = \frac{12 - 0.3}{1000 + 100 + 100K}$$

$$= 0.1157m\text{Amps}$$

Hence, gate voltage is given by

$$V_g = I_c \times 100K\Omega$$

$$= 0.1157m \times 100K$$

$$= 11.57V$$

5.7 Design of the speed sensing unit

The circuit diagram of the speed sensing unit is shown in Fig 5.10. It consists of ILED-photodiode combination to sense the speed.

The disk fitted on the shaft of the motor has single blade. The relative position of the disk and the sensor is so fixed that the blades of disc pass through the ILED-photodiode combination. Each time blade passing though the slot between ILED and photodiode
obstructs the passage of light from LED to photodiode, thereby the photodiode stops conducting and sends the signal to the OPAMP LM348 (acts like a comparator) which drives the transistor and hence the transistor BC 547 goes to cut-off and hence output becomes high (5V). When the blade of disc does not obstruct the light, the photodiode conducts and gives the signal to the comparator which in turn, turns off the transistor. Hence low (0V) voltage is available at the pin no 11 of DSC. A software program is written to calculate the speed on the basis of obstructions per second. The obtained speed is in revolution per second that can be converted in to revolution per minute by multiplying by sixty. Resistance R1 and R3 (1KΩ each) are used to limit the current through ILED and photodiode. R4 (4.7KΩ) is used as base resistance and R5 (1KΩ) is used as collector resistance.

Fig.5.10 Speed sensing circuit
5.8 Conclusion

A closed loop digital controller for the induction motor has been designed using dedicated digital signal controller dsPIC30F2010 IC which includes design of power circuit and control circuit. The main objective of closed loop speed control of induction motor is to maintain the speed of the induction motor constant irrespective of load changes or supply voltage variations. The practical implementation of the developed hardware is discussed in the next chapter.