CHAPTER 1

INTRODUCTION

1.1 GENERAL

System on Chip (SoC) refers to integrating all components of a computer or other electronic systems into a single integrated circuit. It may contain digital, analog, mixed-signal and often radio-frequency function all on a single chip substrate. A typical application is in the area of embedded systems.

Micro-controllers typically have below 100K of RAM (just few Kbytes) and they are really single-chip-systems; where as the term SoC is typically used with more powerful processors, capable of running software such as Windows or Linux which need external memory chip (Flash or RAM) and which are used with various external peripherals. In short, the System on Chip is a hyperbole for larger systems that indicates technical direction more than reality and increasing chip integration will reduce manufacturing costs and enable smaller systems. It is too complex to fit many real time systems on just one chip built with a process optimized for just one of the system’s tasks.

When it is not feasible to construct a SoC for a particular application, an alternative is a System in Package (SiP), which has a number of chips in a single package. In large volume, SoC is believed to be more cost effective than SiP since it increases the yield of the fabrication and its
packaging is simpler. SoC designs usually consume less power and have a lower cost and higher reliability than the multi chip system they replace. And with fewer packages in the system, assembly costs are reduced as well. However like most VLSI designs, the total cost is higher for one large chip than for the same functionally distributed over several smaller chips, because of lower yields and higher design costs (Wael Badawy and Graham Julien 2002).

By the end of the last decade, SoCs, using 50nm nano-transistors operating below one volt, has grown to 4 billion transistors running at 10 GHz, according to International Technology Roadmap for Semiconductors. Caused by steadily increasing number of transistors on a single topology chip, the designers of System on Chip are able to integrate more components like processor cores, DSP cores, memories and specialized hardware on a single chip. The major challenge of the designer of these systems is to provide correct functionality with reliable operation of the interacting components. Moreover, energy and device reliability concerns will impose small logic swings and power supplies, most likely less than one volt (Benini and De Micheli 2002). Electrical noise due to cross talk, electromagnetic interferences, and radiation induced charge induction will likely to produce data errors, also called upsets. On-chip physical interconnections will present a limiting factor for performance and possibly energy consumption and also transmitting digital values on wires will be inherently unreliable and nondeterministic.

The lack of standards and the need for very high performance and reliability, therefore, pushed the development of interconnection networks for multi-computers. Network on Chip (NoC) is such an approach to design the communication system among the Intellectual Property (IP) cores in a System on Chip. NoC applies networking theory and methods to on chip
communication and brings notable improvements over conventional bus and crossbar interconnections. NoCs improve the scalability of SoCs and also the power efficiency of complex SoCs compared to other designs.

Network on Chip is therefore an emerging paradigm for communication within large VLSI systems implemented on a single silicon chip. Network on Chip methodology is therefore called as the layered stack approach to the design of the on-chip intercore communication. In NoC system, the modules such as processor cores, memories and specialized IP blocks exchange data using a “public transportation” sub-system for the information traffic. A NoC is constructed from multiple point-to-point data links interconnected by switches or routers, such that messages can be relayed from any source module to any destination module over several links by making routing decisions at the switches or routers. A NoC is similar to modern telecommunication network, using digital bit packet switching over multiplex links. Although packet-switching is used for a NoC, there are several NoC designs utilizing circuit-switching techniques.

The wires in the links of NoC are shared by many signals. A high level of parallelism is achieved, because all links in the NoC can operate simultaneously on different data packets. Therefore, as the complexities of integrated systems keep growing, a NoC provides enhanced performance and scalability in comparison with the existing communication architecture.

Network on Chip relate closely to interconnection networks for high performance parallel computers with multiple processors, in which each processor is an individual chip. Like multiprocessor interconnection networks, nodes are physically close to each other and have high link reliability. Though it is developed for the demanding communication requirements of multi-computers, Network on Chip is a promising approach to handle these problems by replacing global wires and on-chip buses with packet routing
networks. The main advantages of NoCs are the reduction of electromagnetic effects by introducing structured interconnects layouts with a good scalability and network utilization. The benefits of adopting NoCs are that because of their regular well controlled structure, NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc. An NoC can provide separation between computation and communication, support modularity and IP reuse via standard interface, handle synchronization issues, serve as a platform for system test, and hence, increase engineering productivity (Benini and De Micheli 2002).

The communication in NoCs takes place via data packets, which are delivered between the communicating components. Interconnection networks are currently being used for many different applications, ranging from internal buses in Very Large Scale Integration (VLSI) circuits to wide area computer networks (Duato et al 2003). Among others, these applications include backplane buses and system area networks; telephone switches, internal networks for Asynchronous Transfer Mode (ATM) and Internet Protocol switches, processor or memory interconnects for vector supercomputers, interconnection networks for multi-computers and distributed shared-memory multiprocessors, clusters of workstations and personal computers, local area networks, metropolitan area networks, wide area computer networks and networks for industrial applications. Additionally, the number of applications requiring interconnection networks is continuously growing.

The circuit level, micro-architectural level and system level design techniques developed for the NoCs target a number of performance and cost metrics. The design of the NoCs actually depends on how the topology, the routing protocol and the flow control have been implemented. With the underlying topology as the roadmap, the routing protocol determines the
actual route taken by a packet. The routing protocol is critically important as it impacts all network metrics namely, latency (as the hop count is directly affected by the route), throughput (as congestion depends on the ability of the routing protocol to balance the load), power dissipation (as each hop incurs route energy overhead) and finally reliability (as the routing protocol needs to choose routes to avoid faults). The routing algorithms are of two types: deterministic and adaptive. The deterministic approach routes the packets in the path determined by the source based on the destination address. The adaptive strategy routes the packets based on the status of the network like congestion status, buffer availability etc.

In a practice known as static routing or non-adaptive routing, small networks may use manually configured routing tables. Larger networks have complex topologies that can change rapidly, making the manual construction of routing tables unfeasible. Adaptive routing attempts to solve this problem by constructing routing tables automatically, based on information carried by routing protocols, and allowing the network to act nearly autonomous in avoiding network failures and blockage. Adaptive routing has been employed in multichip interconnection networks as a means to improve network performance and to tolerate network link or router failures (Lee et al 2005, Schonwald et al 2007). Despite additional implementation complexity, adaptive routing is appealing for emerging NoCs with an increasing number of connected elements. Performance can be improved by routing around pockets of congestion and flattening the distribution of traffic among the links. In both cases, the improvement is realized through increased load balance, which smoothes out non-uniformities in the original traffic pattern. However, adaptive routing requires network path diversity between source and destination nodes to facilitate load balance. The availability of network path diversity depends on the topology of the network, the traffic pattern, and whether non-minimal routes are allowed.
Once a path has been established through a router by the switch, messages can be forwarded through the switch. The message forwarding rate is determined by the propagation delay through the switch and the signaling rate for synchronizing the transfer of data between the input and output buffers. Flow control is a synchronization protocol for transmitting and receiving a unit of information. The routing delay and flow control delays collectively determine the achievable message latency through the switch and, along with contention by messages for links, determine the network throughput. The most widely used switching techniques are wormhole switching as it requires small buffers and messages are pipelined through the network. The messages or parts of the messages are buffered at the input and output of each physical channel of the router. A physical channel may support several logical or virtual channels multiplexed across the physical channel. Virtual channels were originally introduced to solve the problem of deadlock in wormhole-switched networks. Virtual channels can also be used to reduce message latency and improve network throughput.

A routing algorithm must strike a balance between the conflicting goals of providing low latency on local traffic and providing high throughput on adversarial traffic. To achieve high performance on local traffic, minimal routing algorithms that choose a shortest path for each packet are favored. Minimal algorithms, however, perform poorly on worst-case traffic due to load imbalance. For an adversarial traffic pattern, a minimal routing algorithm can load some links very heavily while leaving others idle. Non-minimal adaptive routing has the potential to improve load balance beyond the limits of minimal routing, but at the cost of greater implementation complexity and potentially higher per-packet latency and energy. Congestion-oblivious routers are inherently unable to balance the load on many important traffic patterns, because they do not consider the congestion status of available ports. Many congestion-aware routing policies (Hu et al 2004c, Lee et al 2005,
Li et al 2006) have been proposed that route the packets adaptively through the minimal paths. Though the non-minimal routing has greater implementation complexity, it can be employed to analyze the performance of the NoCs when the network is congested.

Network on Chip has been addressed as a solution for both communication requirement and difficulty of global interconnections. The communication in NoC or in Multiprocessor System on Chip (MPSoC) can be either unicast (one-to-one) or multicast (one-to-many) (Lu et al 2006). In unicast a message is sent from a source node to a single destination node, while in multicasting a message is sent from a source node to an arbitrary set of destination nodes. Multicast is an important collective communication operation on multicomputer systems, in which the same message is delivered from a source node to an arbitrary number of destination nodes. Many MPSoC applications such as replication, barrier synchronization, cache coherency in distributed shared-memory architectures, and clock synchronization employ multicast protocol. Although multicast communication can be implemented by multiple unicast communications, this alternative method degrades the performance and increases the congestion in the network (Lin and Ni 1993).

1.2 STATE OF THE ART

The last decade had been the golden era for the interconnection networks research community. Many significant works have been carried out in the area of research in NoCs which greatly impact the performance of the network. Marculescu et al (2005) and Bjerregard and Mahadevan (2006) have discussed the existing works and open research issues under communication infrastructure synthesis, communication paradigm selection and application mapping optimization for the NoCs.
Duato (1993) proposed an adaptive routing algorithm with deadlock-avoidance technique to implement fast hardware router that reduces the communication bottleneck. The deadlock free adaptive routing algorithm was developed for wormhole routers. Two theorems are presented to verify the proposed adaptive algorithm which is deadlock free even when there are cycles in the channel dependency graph. The fault tolerant algorithm is designed with high degree of freedom without increasing the number of physical channels. The algorithm has been evaluated by simulation, showing substantial reduction in message delay as compared with the static algorithm, even with number of virtual channels. The proposed adaptive algorithm scales very well with the network size.

The existing deterministic, partially adaptive and fully adaptive routing algorithms are not completely fault tolerant. Schonwald et al (2007) presented a fully adaptive and fault-tolerant routing algorithm for Networks on Chip. The algorithm is called Force Directed Wormhole Routing (FDWR) because it distributes traffic across the network based on the congestion so that none of the routers in the network are overloaded. It is also made fault-tolerant i.e., ability to re-route dynamically in presence of faulty nodes or links without usage of virtual channels. They have implemented the routers in Transaction Level Model (TLM) which is able to generate switches for different topologies like Mesh, Torus and Hypercube. The simulation results show that whenever the packets take a path that has a faulty router, they are distributed around that router.

Arjun Singh et al (2003) introduced deterministic live lock free routing called Globally Oblivious Adaptive Locally (GOAL) that balances the load globally in the Torus architecture of NoCs. The non-minimal algorithm randomly chooses the direction in which the packets are to be transmitted so that the network is globally balanced. Local load balance is then achieved by
routing in the selected direction adaptively. It has been implemented with the usage of three virtual channels. The authors proved that the GOAL algorithm had better throughput, latency, stability and hot-spot performance compared to the existing algorithms with different traffic patterns. This algorithm shows better performance than the minimal routing algorithms as they route the packets always in the shortest path leaving the other paths idle. The GOAL achieves 58 percent and 76 percent of the throughput of minimal algorithms on nearest neighbor traffic and uniform traffic respectively.

Hu and Marculesu (2004b) presented a novel routing scheme called Dynamic Adaptive Deterministic routing (DyAD) which combines the advantages of both deterministic and adaptive routing schemes. The proposed routing scheme monitors the local traffic of the router and switches to either adaptive or deterministic mode. By default the router functions in deterministic mode and when the network is congested, the router changes to adaptive mode to find the alternate paths thereby leading to high throughput. They have also shown that this approach guarantees freedom from live lock and deadlock situation. The prototype of the DyAD shows that the chip area overhead is marginal (typically less than 7 percent), while its performance consistently outperforms that of a purely adaptive router.

To minimize the implementation cost of the router, it should be implemented with very little area overhead. The input buffers in a typical on chip router take a significant portion of the silicon area of the NoCs. Consequently, their size should be carefully minimized. The performance of a NoC is drastically impacted by the amount of buffering resources it can use, especially when the network becomes congested. Moreover, since the traffic characteristics vary significantly across different applications, the buffering resources have to be judiciously allocated to each input channel in order to match the specific traffic patterns. The uniform distribution of buffering
resources is straightforward and widely used in current NoC designs. But this leads to poor performance and/or excessive use of the silicon area. Hence techniques that utilize the input buffers at the routers based on the characteristics of the application are required.

Hu et al (2004c) presented a buffer allocation algorithm that optimizes the buffer resources at the input channel of the router. The amount of buffers assigned to each input channel is based on the application characteristics that are mapped to the Networks on Chip. The algorithm allocates minimum buffer to the channels and increases the buffer size of the congested channels within buffer limit. Compared to uniform buffer allocation, this algorithm utilizes 85 percent less buffer resources for complex audio/video application. They have also developed a queuing model to quickly analyze the buffer size configuration and detect potential performance bottlenecks in the router channels. The architecture chosen for the study was 2D Mesh with virtual cut-through or store and forward switching. The deterministic routing technique is utilized, as the adaptive routing causes the packets to be delivered out of order.

Ascia et al (2006) proposed new selection policy to exploit the situations of indecision that can occur in an adaptive wormhole routing. The policy can be combined with any adaptive algorithm to avoid deadlock occurrence in the network. A selection strategy is developed with the aim to choose the channel that will allow the packet to be routed to its destination along a path that is as free as possible of congested nodes. The adaptive algorithm with selection policy outperforms the other deterministic and adaptive algorithms with respect to area and power consumption.

The adaptive routing strategies do not deliver the packets in order as it can route the packets in any one of the non-congested paths. Hence the packets have to be reordered at the destination, which is an overhead.
Murali et al (2006) has proposed a routing strategy to optimally spread the traffic in the NoCs. To minimize the network bandwidth requirements and power consumption, the proposed routing strategy delivers the packets in different paths and also maintains the ordering of the packets without any overhead. The multipath routing balances the traffic and shows low power consumption and better throughput. This strategy also supports fault-tolerance with least increase in network traffic. The multipath strategy shows reduction in network bandwidth requirements (36.86 percent on average) and power consumption (30.51 percent on average) than the single path routing schemes.

The routing algorithms are to be designed generic i.e., it can be applied to any topology to improve the performance of the network. The Spidergon network connects a generic even number of nodes $N = 2 \times n$ ($n = 2, 3...$) as a bidirectional ring in both clockwise and anticlockwise directions with an additional cross connection for each couple of nodes. Bononi and Concer (2006) have analyzed the performance of the deterministic routing algorithm in 2D Mesh, Ring and Spidergon architectures. The Spidergon architecture uses simple deterministic routing and wormhole switching. The choice of a deterministic routing and virtual channel scheduling avoids costly disordered end-to-end transfers: the routing path of one packet does not depend on the route of any other packet. The only limitation of this architecture is its implementation cost in terms of silicon area. Abdelkrim Zitouni et al (2007) and Suboh et al (2008) have explored deterministic routing techniques for the Spidergon architecture.

Daneshtalab et al (2007) proposed a routing technique that selects the path based on the load of the neighboring routers. The input selection procedure is based on the priority arbitration policy whereas the output selection is either to the minimal path or non-minimal path. The option of minimal or non-minimal path is decided by circuit arbiter based on the
congestion status provided by downstream routers. The input channel with
higher congestion is given higher priority so that the router efficiency
increases in heavy load traffic. The algorithm shows reduction of power
dissipation to 8 percent.

Adaptive routing algorithms show better performance, increased
throughput and decreased latency compared to the static routing algorithms
under heavy traffic. But the performance is affected when greedy decisions
were made at the router with the local information. Gratz et al (2008) have
shown that when the decisions are made using the local and global
information, the minimal path adaptive routing shows better load balancing in
NoCs. The congestion information is propagated to the neighboring routers.
The local congestion status is aggregated with the global congestion before
propagating to the upstream routers. Since the minimal path is chosen, the
congestion at shorter distance is weighed more than the congestion at a
greater distance.

Suboh et al (2008) have shown that the type of interconnection has
an impact on the performance and area of the Networks on Chip. By
comparison with the other topologies through simulation, they proved that the
Spidergon topology is a good solution from the point of performance and
scalability.

Concer et al (2009) has presented a routing algorithm for the
Spidergon architecture. The AEqualized algorithm balances the traffic around
the hotspot node in the network by choosing either alast or afirst algorithm.
The performance of the network is improved with reduced amount of links
and buffers. Spidergon architecture of NoC always employs deterministic and
shortest path routing algorithms.
Ebrahimi et al (2009) have presented an efficient path-based multicast wormhole routing scheme in 2D Mesh on-chip network which takes advantage of the Odd-Even turn model and congestion detection. In the multicast algorithm, the destination addresses are sorted in a low distance order and then placing this sorted list in the header flit(s) of the message. Afterwards the message is routed towards the destinations such as unicast adaptive wormhole routing which is based on the Odd-Even turn model. The adaptive routing algorithm used the congestion condition of the input ports to route messages through non-congested paths so that load is balanced uniformly in the network.

Moadeli et al (2007) have presented a novel analytical model to compute communication latency of multicast as a widely used collective communication operation. They have predicted the latency of the multicast communication in wormhole routed architectures by employing asynchronous multi-port routers scheme. The analytical model had been applied for Quarc architecture of Networks on Chip and validated with the simulation results.

Moadeli et al (2010) have presented an analytical performance model for the Spidergon NoC. They analyzed the impact of virtual channels on the performance of the network. To date, several prototype NoCs have been designed and analyzed in both industry and academia but only few have been implemented on hardware. However, many challenging research problems remain to be solved at all levels, from the physical links through network level, and all the way up to the system architecture and application software. Yet works are to be carried out to explore congestion-aware routing strategies that are adaptive and fault tolerant.
1.3 OBJECTIVES

The need for robust and reliable communication grows as parallel computing architectures grow in size and find their way into mission-critical applications. The main objective of this research is to develop a reliable and congestion-aware adaptive routing model to improve the performance of the Networks on Chip. Compared to a standard data macro network, an on-chip network is by far more resource limited. Buffers are one of the major resources used by the routers in virtual channel flow control. It is reported that they consume 60 percent of router’s silicon area. Architects of interconnection networks must therefore use the buffers efficiently while assigning buffers to virtual channels from the fixed buffer capacity. Normally uniform allocation is used which reduces the performance or increases the excessive usage of the silicon area. Moreover, since the traffic characteristics vary significantly across different applications, the buffering resources have to be judiciously allocated to each input channel in order to match the specific communication patterns.

Many of today’s NoCs designs are based on minimal path routing taking into account of only local congestion information. The major problem with the routing based on local congestion information is that the packet delivery gets disrupted in case of higher percentage of load and results to higher latency and lower throughput and the performance of the whole system gets reduced.

A well-designed wormhole 2D Mesh router should support native multicast, adaptive routing, fault tolerance and deadlock free so that packets can be routed efficiently. Unfortunately, most wormhole routers exhibit only a subset of these characteristics. Currently, there exists a virtual cut-through router that supports all of these characteristics. The main disadvantage of a virtual cut-through router is its higher buffer requirements. In a virtual cut-
through router, each buffer should be large enough to store the whole packet. In an area constrained on-chip network, buffer size is usually small. Therefore, virtual cut-through routing restricts the network to use short packets.

The performance of wide range of on-chip network applications demands adopting different architectures suited for an application. However, there are a number of methods and techniques that are widely employed to improve the performance of a topology. The main driving factor in the current research activity of the Spidergon topology is to explore the complex design space to match a low cost hardware implementation.

Specifically, the objectives of this research are detailed as follows:

- To propose buffer allocation algorithm that allocates the buffer for each input channel based on the application requirements within the total buffer capacity to avoid congestion
- To implement an enhanced adaptive strategy to avoid congestion and also balance the load in the network based on the local and global network congestion status
- To explore the performance of the fault-tolerant adaptive routing for the Spidergon architecture of Networks on Chip
- To analyze the performance of the fault tolerant and adaptive turn routing model for multicast strategy
1.4 SCOPE OF THE THESIS

The thesis entitled “Enhanced and Reliable Adaptive Routing Models for Networks on Chip” delineates the development of enhanced routing models to avoid congestion, improve performance under different traffic patterns and to make the on-chip networks fault-tolerant. This dissertation is divided into five chapters including this introduction chapter.

Chapter 2 brings out the architecture and components of abstract router of the on-chip networks. The various switching techniques employed in Networks on Chip are reviewed. The wormhole switching technique is most widely used compared to virtual cut-through or store and forward switching. The wormhole switching requires small buffers as the packets are split into flits. The classification and the different implementations of the routing algorithms are discussed. The cause of the congestion and its impact on the performance of the on-chip network are discussed. The congestion control mechanisms like increasing the number of virtual channels, inclusion of extra hardware are reviewed. Another solution to congestion avoidance is adaptive routing which can provide multiple paths between a source and destination. There exists a variety of SoC applications like multimedia processing that necessitates supporting multicast. Support of multicast increases the deadlock situation and network congestion thereby degrading performance. Fault tolerance and performance are two important problems that should be addressed. The current generation of fault-tolerant routing algorithms is covered in this chapter. The routing models that avoid congestion and realize fault-tolerance without performance degradation are also discussed and their significance is emphasized.

Chapter 3 discusses the buffer allocation algorithm to deal with the congestion avoidance in the Networks on Chip. A deterministic routing that allocates the buffer dynamically for the wormhole router is presented in this
chapter. This work proposes a dynamic buffer allocation algorithm that automatically assigns the buffer depth for the input channels of the routers in the network in order to match the specific communication patterns that characterize various applications. A Queuing model M/M/1/K is used for modeling the arrival rate of the flits, the blocking probability and the service rate of each input channel. Since in wormhole routing, each packet is split into flits, each flit that arrives at each channel is assumed to be the customer in the Queuing model. The packet injection rate, blocking probability and service rate of each input channel are studied and presented in this chapter. An efficient Greedy algorithm is proposed, which automatically allocates the buffering resources to different NoC channels, such that the communication performance is improved while satisfying the total buffering resource capacities.

In this chapter, a fully adaptive and fault-tolerant Multi-Path based multicast routing model has been proposed and the performance is compared with the existing unicast algorithms. The adaptive strategy is based on Odd-Even model that considers congestion in the neighbouring nodes to decide the direction of output port to route the packets. The proposed Multi-Path based multicast scheme is made fully adaptive by allowing packets to take a prohibited turn in case of link failure, with help of an additional buffer called Deadlock Avoidance Data Buffer, thus making the NoC fault tolerant. The algorithm has been simulated using Nirgam simulator and it shows better performance as the injection rate increased with faulty links in the network.

Chapter 4 deals with the implementation of enhanced adaptive router architecture and the algorithm that considers local and global congestion status to select the path to destination. It also balances the traffic in the network in the presence of faulty links or nodes. The proposed enhanced routing strategy routes the packets using non-minimal path between
the source and the destination instead of the minimal path. This helps in reducing the latency of the whole network because the minimal path considered may have more congestion when compared to the other non-minimal paths. Since non-minimal paths are considered, the packets can be routed through other paths which have lower congestion. In this strategy, the routing algorithm routes the packets based on global network information along with the status of the neighboring nodes. Thereby it balances the load across the network and the latency is reduced. Hence a design methodology is developed which has better fault tolerance characteristics, better network throughput, and decreased latency compared to oblivious policies when faced with non-uniform or bursty traffic. This algorithm can be extended to various other topologies with different traffic patterns.

In this chapter, a fault-tolerant adaptive routing called Dynamic Stress Wormhole Routing (DSWR) for Spidergon architecture is presented. When the routers or links fail, the routing scheme routes the packets in an alternate path to the destination. In the presence of congested nodes called hotspot nodes, the traffic load is balanced across the network. A study of the impact on the latency is made using the dynamic routing strategy with load balancing for the Spidergon architecture of NoC. The evaluation of the adaptive routing is made using two virtual channels. The implementation of the enhanced routing strategy and fault tolerant adaptive routing are also discussed and the results are compared with the deterministic routing algorithm. Any real time application can be mapped to a Spidergon architecture to study the performance of DSWR algorithm.

In Chapter 5, a review of the work reported and the contributions made are dealt with. The developed routing models are fault-tolerant and adaptive with load balancing capability. Recommendations for future research are stated.