Preface

The scaling of advanced MOS technology is now entering the region of its limits. When MOS technology was developed in the 1960’s, channel lengths were about 10 micrometers, but researchers are now building transistors with channel lengths of less than 10 nanometers. As the scaling extends to the region below the quantum-size criterion, it should be noted that the original optical, electrical, thermal, and chemical properties of bulk silicon are substantially modified. This thesis focuses on the charge transport through a nano electronic device such as DG MOSFET when a voltage is applied across it. This is a problem of great practical importance as devices like transistors get downscaled to nano dimensions.

In the first two chapters, the problem and the method of analysis of quantum transport in nanoscale DG MOSFET are presented. The short channel effects of ultrascaled device are discussed. The non equilibrium Green’s function (NEGF) formalism which is the method of analysis is explained utilizing the physics of quantum transport, developed by Keldysh and reformulated by Datta. The algorithm of numerical method is explained in brief. Various approaches to solve the NEGF equation, based on real space and mode space
approximation are discussed in brief. This is followed by discussion on the method of further calculations of short channel effects like, threshold voltage \( V_T \) roll-off and drain induced barrier lowering (DIBL), subthreshold leakage current and subthreshold swing (SS).

The next five chapters present the application of the methodology of simulation discussed before, to various aspects of DG MOSFETs. The influence of channel length \( L_g \) and channel thickness \( T_{Si} \) on nano DG MOSFETs are discussed. Optimization of device parameters for 10 – 26 nm channel length range are also attempted. Influence of variation of counter-doping thickness on nano DG MOSFETs are discussed. The counter doped (p–type) DG MOSFETs with high–κ gate dielectric material are modeled to obtain the transport characteristics and the short channel effects are estimated. The counter doped (p–type) DG MOSFETs with different metal gate work functions are simulated to obtain the transport characteristics and short channel effects (SCF). Split gate structure, SCE suppression and device performance by combinations of split metal gate materials are discussed.

Finally, the last chapter is the conclusion of the thesis.