Chapter 7

Effect of Split Gate in DG MOSFETs

7.1 Introduction

As discussed in the last chapter, the threshold voltage of the DG MOSFET is dominantly determined by the work function of the gate material; it is possible to avoid channel doping and associated fluctuation effects [78]. DG MOSFET with two different gate work functions is required to reduce the bottleneck barrier length to enhance the ballisticity due to inelastic phonon emission. It has been reported that source–end potential engineering is effective in achieving ballistic current in Si MOSFETs [95]. In an earlier work, Deepanjan et al. [96] reported that nanoscale parallel connected heteromaterial double gate (PCHEM-DG) architecture with triple metal gate which significantly suppresses band to band tunneling (BTBT) leakage, making it efficient for low power very large scale integration (VLSI) design in the sub-10 nm regime.

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In this chapter, split metal gate combinations of Ta, Al and TaSiN, dielectrics such as SiO$_2$, HfO$_2$ and undoped channel, were considered in computation of the quantum transport current in DG MOSFET with physical oxide thickness 1 nm. Two dimensional quantum transport equations and Poisson equations are used to compute DG MOSFET characteristics self-consistently. In this study DG MOSFET with the following split-gate configurations has been considered:

- The work function of metal gate I at both ends are lower than metal gate II i.e., $\phi_I < \phi_{II}$
- The work function of metal gate I at source side is lower than metal gate I at drain side i.e., $\phi_S < \phi_D$
- Uniform metal gate (Al)
- The work function of metal gate I at source side are greater than metal gate I at drain side i.e., $\phi_S > \phi_D$
- The work function of metal gate I at both ends are greater than metal gate II i.e., $\phi_I > \phi_{II}$

The objective of this work is to investigate the potential benefits offered by the split gate in suppressing the short channel effects in DG MOSFETs 7.1.

### 7.2 High–$\kappa$ Gate Dielectrics and Split Gate

The introduction of high–$\kappa$ gate dielectrics and metal gates reduce gate insulator tunneling by several orders of magnitude and renew device length scaling.
7.2 High–κ Gate Dielectrics and Split Gate

Figure 7.1: A double gate MOSFET structure with split gate work functions in both top and bottom of the gate dielectric. Where metal gate lengths $L_{gI} = 3$ nm and $L_{gII} = 4$ nm are used in all our simulation.

Feature size tolerance issues then become the ultimate limit to scaling, presenting profound limitations at the 22 nm node [97]. The use of a high–κ gate dielectric between the metal gate and the III–V semiconductors device layers will eliminate such leakage and potentially improve the $I_{on}/I_{off}$ ratio. The thinner gate oxide leads to an exponentially increased leakage current due to direct tunneling through the dielectric. The higher effective channel doping degrades the carrier mobility and increases source/drain junction leakage. The higher channel doping also induces doping fluctuation, and thus threshold voltage variation in the nanoscale transistor [98]. To overcome the above issues, the mobility enhanced technology and high–κ / metal gate are introduced to improve the ON state drive current without degrading OFF state leakage current. The $V_T$ may be lowered while providing significantly better subthreshold characteristics by using a refractory metal gate such as tungsten or tantalum. Low power applications such as battery operated hand held devices require a
reduced gate leakage current. To reduce the gate leakage, standard oxynitride gate insulators will be replaced by high-$\kappa$ dielectrics. Among the promising candidates for the 45 nm technology node are hafnium oxides (HfO$_2$) and hafnium silicates HfSiON with a high-$\kappa$ value in the range 10-15, which should be compared to 3.9 for SiO$_2$ and 6-7 for the oxynitrides.

Use of the high-$\kappa$ dielectric will allow a less aggressive gate dielectric thickness reduction while maintaining the required gate overdrive (gate voltage minus threshold voltage) at low supply voltages. When the gate overdrive diminishes, it will lead to a reduction in the drain current. As the physical gate length is scaled, ideally the gate dielectric equivalent oxide thickness is also scaled correspondingly to control short channel effects and to increase the saturation current drive. Using high-$\kappa$ dielectric, the physical thickness of the dielectric layer can be kept large, thereby reducing the gate leakage current, while maintaining the same value of capacitance [70]. There are many materials systems under consideration which have potential to replace SiO$_2$ as the gate dielectric material. Of the various high-$\kappa$ dielectric materials, SiO$_x$N$_y$, Al$_2$O$_3$, HfO$_2$, La$_2$O$_3$, and ZrO$_2$ have generated a lot of interest due to their high dielectric constant and adequate barrier height [71].

The threshold voltage ($V_T$) depends not only on the gate work functions, but also on the silicon and gate oxide thicknesses [80]. In order to tailor the $V_T$, it is important that the gate material should have a tunable work function [81]. A key technological challenge for DG MOSFET is to find gate materials with proper work functions for the desired threshold voltages [82]. Therefore, a gate material with a work function that places its Fermi level close to the middle of the silicon band gap is desired so that the work function difference
between the gate electrode and the near intrinsic silicon film can be adjusted to optimize the threshold voltages. At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film [78]. To control the threshold voltage of MOSFETs, heavy body doping is not compatible with the fully depleted body design which suppresses the floating body effect, improves mobility, and suppresses the dopant fluctuation effect. The threshold voltage requirements pose a severe challenge to the process technology for appropriate gate materials with the tunable work functions that would be compatible with the CMOS process. The threshold voltage can be tuned by the silicon body thickness and the gate work function without substrate doping [83, 65].

7.3 Method of Analysis

For the high-κ dielectric materials, in the absence of reliable reference data, effective mass of electrons in dielectric $m_{ox}$ is still widely treated as a fitting parameter and is taken as in gate dielectric region by a constant $m_{ox}$. Effective electron mass in the gate dielectrics is assumed to be equal to 0.5 $m_e$ and 0.32 $m_e$ for 1 nm and 2 nm gate oxide thickness, where $m_e$ is the free electron mass [76, 77]. Conduction band offset to silicon $\Delta E_c$ (eV) and dielectric constant ($\epsilon_r$) of the HfO$_2$, dielectric material used for this computation are 1.5 eV and 20 respectively [90, 91, 92, 93, 94].

The method of numerical simulation is the same as described in chapter 2. Silicon dioxide is used as a gate dielectric due to its electrical isolation in
a SiO$_2$–Si based structure. This electrical isolation is due to the relatively large band gap of SiO$_2$ (9 eV), making it a good insulator. Although different high–κ dielectric materials are characterized by different values of conduction (valence) band offsets with silicon $\Delta E_c(\Delta E_v)$, dielectric constant ($\epsilon_r$), and electron effective mass in dielectric region $m_{ox}$, combined effects of these parameters through wave function penetration on gate are taken into this computation. In order to get the actual influence of high–κ dielectric material in DG MOSFETs characteristics, we used physical dielectric thickness of 1 nm for all computations instead of effective oxide thickness. If the comparison is done with effective oxide thickness, effect of high–κ dielectric is not reflected in the DG MOSFET characteristics.

7.4 Results and Discussion

Output characteristics of the undoped DG MOSFET having channel length $L_g (L_{g1} + L_{gII} + L_{gI}) = 10$ nm, where metal gate lengths $L_{gI} = 3$ nm and $L_{gII} = 4$ nm, $T_{Si} = 3.2$ nm and $T_{ox} = 1$ nm with dielectric SiO$_2$/HfO$_2$ and split metal gate combinations of Ta, Al and TaSiN are shown in Figs. 7.2 and 7.3.

We observe that, the drain current current decrease as we change the combination of split gate metal except that the Ta Al TaSiN combination (see Figs. 7.2 and 7.3, curve b). The split gate device demonstrates excellent current saturation compared to low dielectric DG MOSFET (see Fig. 7.3).

Figures 7.4 and 7.5, curves a to e show that the decrease in subthreshold leakage current is observed with higher metal work function at source and drain ends. The result shows that the split gates are needed to minimize the source
to drain subthreshold leakage current when incorporating high–κ dielectrics.

Lifting of first subband energy at source side along the length of the channel with the increase in metal work function $\Phi_I$ at both ends (source and drain) is observed in Fig. 7.6 and 7.7 (curves a to e). This is due to the increased electric field within the oxide region influencing the potential inside the channel. Lifting of potential profile due to the increase in metal work function $\Phi_I$ at both ends leads to lowering in electron density in the channel as shown in Figs. 7.8 and 7.9. The potential is allowed to float to any value it chooses to satisfy the charge neutrality. So in this case, the potential is lifted to decrease the electron density. Split gate in DG MOSFET leads to a simultaneous transconductance enhancement and suppression of short channel effects due to the modified potential function in the channel. It is evident from
Figure 7.3: Output characteristics of the split gate DG MOSFET device, with $T_{ox}=1 \text{ nm}$, $T_{Si}=3.2 \text{ nm}$, $L_g (L_g+L_{gII}+L_{gIII})=10 \text{ nm}$ and HfO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.

Table 7.1: Comparison of subthreshold slope(SS), Threshold Voltage ($V_T$) and $I_{on}/I_{off}$ variation between Split gate DG MOSFETs by dielectric SiO$_2$ and HfO$_2$ (values in bracket).

<table>
<thead>
<tr>
<th>Split Gate</th>
<th>SS (mV/dec)</th>
<th>$V_T$ (Volt)</th>
<th>$I_{on}/I_{off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ta Al Ta</td>
<td>116 (92)</td>
<td>0.332 (0.416)</td>
<td>1.19E+03 (1.06E+05)</td>
</tr>
<tr>
<td>Ta Al TaSiN</td>
<td>103 (118)</td>
<td>0.338 (0.419)</td>
<td>1.97E+03 (2.70E+05)</td>
</tr>
<tr>
<td>Al</td>
<td>104 (144)</td>
<td>0.347 (0.443)</td>
<td>1.97E+03 (1.97E+05)</td>
</tr>
<tr>
<td>TaSiN Al Ta</td>
<td>119 (121)</td>
<td>0.350 (0.431)</td>
<td>1.92E+03 (2.95E+05)</td>
</tr>
<tr>
<td>TaSiN Al TaSiN</td>
<td>107 (92)</td>
<td>0.365 (0.452)</td>
<td>4.29E+03 (4.72E+05)</td>
</tr>
</tbody>
</table>
Figure 7.4: of transfer characteristics of the split gate DG MOSFET device, with $T_{ox}=1$ nm, $T_{Si}=3.2$ nm, $L_g=10$ nm and SiO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.

Our results displayed in Fig. 7.8 and 7.9, that the lowering in electron density at source end is higher for high–$\kappa$ dielectric materials compared to SiO$_2$.

At very short gate length, the DG MOSFET device operation is asymmetrical even at very small drain bias due to a higher drain side electric field resulting in short channel effects. Unconventional asymmetrical structures have been employed to reduce the drain side electric field and its consequent impact upon the channel. Split gate structure offers an alternative way of SCE suppression and improved device performance by combinations of split metal gate materials. Split gate structure employing gate material engineering with different work functions introduces a potential variation along the channel. This leads to a suppression of SCEs and an enhanced source side electric field resulting in increased carrier transport efficiency in the channel region.
Figure 7.5: Transfer characteristics of the split gate DG MOSFET device, with $T_{ox}=1 \text{ nm}$, $T_{Si}=3.2 \text{ nm}$, $L_g=10 \text{ nm}$ and HfO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.

The device subthreshold swing (SS), threshold voltage ($V_T$) and $I_{on}/I_{off}$ for different split gate DG MOSFETs are given in Table 7.1. High–κ devices can be scaled to shorter lengths than those with an SiO$_2$ gate dielectric without important characteristics such as $I_{on}/I_{off}$ and subthreshold swing are degraded. In addition, this split gate structure reduces the subthreshold swing (SS), increases on–off current ratios, decreases the subthreshold leakage current and suppresses the short channel effects. The $I_{on}/I_{off}$ ratio of $10^5$ is obtained with high–κ device, as the key parameter for device operation.
Figure 7.6: subband energy vs position along the length of the split gate DG MOSFET device, with $T_{ox}=1$ nm, $T_{Si}=3.2$ nm, $L_g=10$ nm and SiO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.
Figure 7.7: subband energy vs position along the length of the split gate DG MOSFET device, with $T_{ox}=1$ nm, $T_{Si}=3.2$ nm, $L_g=10$ nm and HfO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.
Figure 7.8: 2D Electron density vs position along the length of the split gate DG MOSFET device, with $T_{ox} = 1$ nm, $T_{Si} = 3.2$ nm, $L_g = 10$ nm and SiO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.

Figure 7.9: 2D Electron density vs position along the length of the split gate DG MOSFET device, with $T_{ox} = 1$ nm, $T_{Si} = 3.2$ nm, $L_g = 10$ nm and HfO$_2$ gate dielectric, (a) Low metal gate work function (Ta=4.2 eV) at both end, (b) Low metal gate work function (Ta) at source end, (c) Constant metal gate work function (Al=4.28 eV), (d) High metal gate work function (TaSiN=4.4 eV) at source end and (e) High metal gate work function (TaSiN) at both end.
7.5 Summary

Split gate structure offers an alternative way of suppressing short channel effects and improved device performance by combinations of split metal gate materials. The split gates are needed to minimize the source to drain sub-threshold leakage current when incorporating high–\(\kappa\) dielectrics. The split gate device demonstrates excellent current saturation compared to low dielectric DG MOSFET. High–\(\kappa\) devices can be scaled to shorter lengths than those with an SiO\(_2\) gate dielectric without important characteristics such as \(I_{on}/I_{off}\) and subthreshold swing (SS) are degraded.