Chapter 4

Counter Doped DG MOSFET

4.1 Introduction

In bulk MOSFETs, counter-doping is used at the surface to obtain low threshold voltages [64]. However, as a method to adjust the threshold voltage, undoped DG MOSFETs need to rely on gate work function to achieve multiple threshold voltages on a chip, but metal gates with work functions lower than that of $n^+$ Si are not available [64, 65]. In this chapter, we are studying the possibility of adjusting threshold voltages of DG MOSFETs by varying the thickness of counter-doping (means n or p type doped thin layer) layer located within a thin layer of $n^+$ or $p^+$ doped Si below and above the insulator. We have studied the effect of counter doping thickness variation on the short channel effects. n type and p type doping have been simulated. Increase in p-type counter-doping thickness improves $V_T$, and improves substantially the subthreshold slope compared to the n-type counter-doping thickness.
4.2 Computational Procedure

The structure of the DG MOSFET considered in this chapter is schematically presented in Fig. 4.1. This symmetric structure is characterized by two identical gates with no overlap with the source/drain extensions.

We assume a metal gate contact Aluminum(Al) with work function 4.28 eV and 1 or 2 nm thick layers as the top and bottom gate dielectric. The source and drain regions included in the finite difference simulation grid are 3.2 nm in extension and have a uniform doping of $10^{20}$ cm$^{-3}$. The channel is made up of counter-doped layers with doping concentration $10^{19}$ cm$^{-3}$ and undoped Si layer for all devices simulated. The channel length is 10 nm and channel thickness is varied from 2.2 nm to 3.2 nm in steps of 0.5 nm for studying the variation of DIBL, drain current, threshold voltage and subthreshold swing.

![Figure 4.1: A double-gate MOSFET structure with counter-doping. The 2D simulation domain is the portion excluding the top and bottom rectangles marked as ‘Gate’.](image)
with change in thickness of counter-doping ($T_C$).

The effective mass equation is solved in two dimensions, a 2D solution to the Schrödinger equation is obtained by solving two 1D problems, one in the direction normal to the channel, which yields the vertical electron concentration and subband profiles, and the other, along the channel direction based on the subband profiles yielding the electron concentration in the transmission direction. The physics of carrier transport along the channel direction, uses the Green’s function formalism. A 2D Poisson solver is coupled to the ballistic transport models to provide self-consistent solutions. The electrostatic effects due to penetration of the electron wave functions into the oxide regions are accounted for in our simulations by extending the quantum solution domain to include the these regions.

4.3 Results and Discussion

4.3.1 Current Characteristics

Drain and Subthreshold characteristics of the counter doped DG MOSFET having channel length ($L_g$) = 10 nm, channel thickness ($T_{Si}$) = 3.2 nm, $T_C$ = 0.2 to 1 nm and $T_{ox}$ = 2 nm with drain voltage ($V_{ds}$) = 0.6 V are shown in Fig. 4.2.

From the Fig. 4.2 ON current decreases with the increase in counter p-type doping thickness and ON current increases with the increase in counter n-type doping thickness, it is clear from the Fig. 4.3 that the subthreshold leakage current ($I_{off}$) decreases with the increase in counter p-type doping thickness and subthreshold leakage current ($I_{off}$) increases with the increase in counter
Figure 4.2: Comparison of the Drain characteristics for the counter doped DG MOSFETs with different counter doping thickness (n-type and p-type) n-type doping thickness.

4.3.2 Local Density of States (LDOS)

Figure 4.4 shows local density of states in the DG MOSFET. Several quasi-bound states are seen in the device. In the second subband, negligible amount of carriers exist. Tunneling through the potential barrier at the source end and quantum interference in the device are clearly observed. Carriers flow not only in the lowest subband but also in the second lowest one around the drain region, which cannot be expressed in conventional quantum correction methods. The subband energies become closer when the channel thickness increases from 2.2 nm to 3.2 nm resulting reduction in the subthreshold leakage current (see Fig. 4.4, a, b and c). Spreading the subband energy and of LDOS is observed by counter doping (p-type) of the channel (see Fig. 4.4, d, e and f).
4.3 Results and Discussion

Figure 4.3: Comparison of the Subthreshold characteristics for the counter doped DG MOSFETs with different counter doping thickness (n-type and p-type)

4.3.3 Short Channel Effects

The DIBL is calculated from the computed values of $I_{ds}$ and $V_{gs}$ for different counter-doping thickness and are plotted in Fig. 4.5.

It is observed that as $n^+$ counter-doping thickness increases, DIBL increases slightly. The DIBL value remains almost same when there is increase in $p^+$ counter-doping thickness.

Figure 4.5 shows the subthreshold slope as a function of the counter-doping thickness at different (2.2, 2.7 and 3.2 nm) channel thickness. Increase in n-type counter-doping thickness of DG MOSFET exhibits slight subthreshold slope degradation. But in the case of p-type counter-doping, the subthreshold slope improves substantially compared to the n-type counter-doping. It is of significant importance to reduce the subthreshold swing, which is a measure
of the rate of change in current ($I_{ds}$) as a function of gate voltage ($V_{gs}$) in a MOSFET, since a lower subthreshold swing will lower the supply voltage and hence the dissipation. As can be seen from Fig. 4.5, the n-type counter-doping thickness slightly reduces the threshold voltage.

However, a reduction in the threshold voltage gives rise to an increase in the subthreshold leakage current, which is the current that is conducted through a transistor from its source to drain when the device is intended to be off. Due to this increase in subthreshold current, static power consumption is increased. In contrast, increase in p-type counter-doping thickness improves $V_T$ and the subthreshold slope improves substantially compared to the n-type counter-doping thickness. Increasing the threshold voltage of the DG MOSFET is an effective way to reduce subthreshold leakage.

### 4.3.4 Transconductance and Drain Conductance

Transconductance, $g_m$, is a measure of the sensitivity of drain current to changes in gate–source bias. The barrier width is modulated by the application of gate voltage and thus the transconductance of the device is dependent on the gate voltage. The transconductance $g_m$ is extracted from the slope of $I_{ds} - V_{gs}$ from $V_{gs}=0$ to .6 V at $V_{ds}=0.6$ V. The transconductance is plotted with different channel thickness $T_{Si}$, 2.2, 2.7 and 3.2 nm as shown in Figs. 4.6 and 4.8.

The transconductance increases with increasing counter-doping thickness of DG MOSFET. One of the most remarkable results in this work is the very high transconductance ($\approx 40mS/\mu m$) observed for the 10 nm channel length DG MOSFET.
4.4 Summary

The drain conductance $g_d$ is extracted from the slope of $I_{ds} - V_{ds}$ from $V_{ds}=0$ to .6 V at $V_{gs}=0.6$ V. The drain conductance of the p-type counter-doped devices improve as compared to the undoped channel (see Figs. (4.7 and 4.8)).

**4.4 Summary**

We have investigated the variation of important short channel effects, DIBL and subthreshold swing, in counter-doped DG MOSFETs. P-type 0.6 nm counter-doped channel devices with channel thickness 3.2 nm, channel lengths of 10 nm and gate oxide thickness of 1 nm show transconductance of 40 $mS/\mu m$, subthreshold slope of 102 mV/dec and DIBL of 89 mV/V and threshold voltage of 0.302 V. Increasing the threshold voltage of the DG MOSFET is an effective way to reduce subthreshold leakage and DIBL. Increase in p-type counter-doping thickness improves $V_T$, and improves substantially the sub-threshold slope compared to the n-type counter-doping thickness. Therefore, counter-doping thickness can be used as an alternative to achieve multiple threshold voltages on a chip.
Figure 4.4: Computed local density of states (LDOS) of DG MOSFET along X direction in the on state. Broadening in the LDOS is due to quantum mechanical coupling to the S/D and oscillations are due to the quantum mechanical reflection. Where $L_g = 10$ nm (a) $T_{Si} = 2.2$ nm (b) $T_{Si} = 2.7$ nm (c) $T_{Si} = 3.2$ nm (d) $T_{Si} = 2.2$ nm and $T_C = 0.6$ nm (e) $T_{Si} = 2.7$ nm and $T_C = 0.6$ nm (f) $T_{Si} = 3.2$ nm and $T_C = 0.6$ nm
Figure 4.5: (A) DIBL as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm \((n^+\) type) and (d) 3.2 nm \((p^+\) type), (B) Subthreshold swing as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm \((n^+\) type) and (d) 3.2 nm \((p^+\) type) and (C) Threshold voltage as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm \((n^+\) type) and (d) 3.2 nm \((p^+\) type)
Figure 4.6: Transconductance curve computed for undoped and counter doped channel, $T_{Si}(A)$ 2.2 nm, (B) 2.7 nm and (C) 3.2 nm.
Figure 4.7: Drain Conductance curve computed for undoped and counter doped channel, $T_{Si}$ (A) 2.2 nm, (B) 2.7 nm and (C) 3.2 nm.
Figure 4.8: (A) Transconductance curve computed for undoped and counter doped channel, (a,d) 2.2 nm, (b,e) 2.7 nm and (c,f) 3.2 nm, (B) Drain conductance curve computed for undoped and counter doped channel, (a,d) 2.2 nm, (b,e) 2.7 nm and (c,f) 3.2 nm.