CHAPTER - 7

CONCLUSION AND FUTURE SCOPE

CONCLUSION

In this work, a technique was presented to create an “agent” based framework for the NOC implementation.

- This is an attempt to get rid of external routers and allow the data communication to happen from an external layer of the processing elements.
- The systems route the packets with the awareness of the state of the neighboring elements.
- It can also be noted that this framework is suitable for heterogeneous implementation of NOCs as well.
- The data integrity issues are well handled by framing data along with appropriate headers.
- The FIFOs are also used to handle data rate mismatch issues.
- We have designed the PEs to be self-contained so that they can be individually controlled.
- This helps in scalability and when not required they can be turned off so that power can be saved.
- This will also allow the scale-up and scale-down of the system with ease.
- This is because the strategy of the NOC should be made available for all families of the FPGAs small or big.
- Multi-port top level packet injection allows the quick transfer of packets into the networked processing elements.
With The Implemented Architecture, Area decreased by 35%, Speed increased by 25%, Throughput increased by 18% and Delay decreased by 12%.

FUTURE SCOPE OF THE RESEARCH

• Future work should involve testing the network for different loads and studying the performance of the design for various applications.

• Fault tolerance capability can also be included in the design. This should give way to an improvised scalable networking mechanism on chip.

• Apart from these, it is also foreseen through intuitive analysis that several other issues can be addressed such as
  
  o A deeper study on the impact of the state of neighboring elements on routing.
  o Scale-up modality.
  o Timing closure for FPGA and ASIC implementation.
  o Deadlock recovery.
  o Load balancing.
  o Energy factor etc.

Summarize the advantages:

• Better throughput.
• Improvement in working frequency on various FPGA families.
• Scalable and upgradable.
• Works both in heterogeneous and homogeneous modes.
• Global transmission lines transport packets easily to processing elements at farther ends.
• Adaptive packet routing in-built into the processing element.
- Minimized dead locks.
- Better load balancing.
- Re-sizeable to suit multiple families of FPGA including small FPGAs.
- Minimized connections improve power utilization.
- Better handling of unprocessed packets.
- Capable of working in mixed range of operating frequencies, i.e. each element can work in a different frequency.
- Practically implementable on an FPGA, not just simulation.
- Logic utilization is improved in FPGAs.
- Protocol oriented data transfer help data integrity.