CHAPTER 4

NANOSCALE DG MOSFETs USING HIGH-K DIELECTRICS

4.1. INTRODUCTION

CMOS technology has seen excellent high-speed performances achieved through improved design, use of high quality materials and processing innovations over the past decade. Further, the advancement in CMOS technology has made it also attractive for System-on-Chip (SoC) applications where the analog circuits are realized with the digital circuits in the same integrated circuit in order to reduce the cost and improve the performance (Chakraborty et al 2007). The primary driver of the exponential improvements in integrated circuit performance has been the scaling of MOSFET dimensions. However the continuous scaling of MOS device has led to many challenges such as diminishing gate control over the channel, resulting in increased short-channel effects (SCEs) and high Off current. The DG MOSFETs termed as FinFETs provides better scalability option due to its excellent immunity to SCEs, higher drive current and transconductance, lower Off current and better scaling capability compared to the bulk MOSFETs. The presence of second gate increases the effective gate control and reduces the DIBL (Manoj et al 2007).

For the past many years the physical thickness of SiO$_2$ has been aggressively scaled for low-power, high performance CMOS applications. This continuous down scaling of CMOS devices into deep sub-micrometer dimensions seems to have reached its limits with SiO$_2$ as the gate dielectric material. However continual gate oxide scaling, will require the use of dielectric materials with higher dielectric constant, since the gate oxide leakage is increasing with decreasing SiO$_2$ thickness, and also SiO$_2$ is running out of atoms for further scaling (Wilk et al 2001). So in order to improve the device performance, high-k materials are used as gate dielectrics in devices instead of SiO$_2$. High-k dielectric materials have equivalent oxide thickness (EOT) of 1.0 nm with negligible gate oxide leakage, desirable transistor threshold voltage for MOSFETs, and transistor channel mobility close to
those of SiO$_2$. Possible high-k materials are Si$_3$N$_1$ (k~7.5), Al$_2$O$_3$ (k~10), LaAlO$_3$ (k~15), HfO$_2$/ZrO$_2$ (k~25), La$_2$O$_3$ (k~27), TiO$_2$ (k~40). In the previous chapter it is shown that ZrO$_2$ is one of the best alternate high-k gate materials which provide lesser physical thickness, since it is a nano sized material and reduces the direct tunnelling Off current. Even though TiO$_2$ has high dielectric constant value of 40, the band gap offset is very low as (~3 eV). So the Off current is more for TiO$_2$ as a gate material in DG MOSFET (Rajesh Kumar et al 2011).

DG MOSFETs are used for CMOS applications beyond the 45 nm node of the SIA roadmap because of their excellent scalability and better immunity to short channel effects. The device performance is analyzed by replacing the SiO$_2$ with various high-k materials and the gate oxide thickness is scaled so that they have the same EOT. This chapter explains about the impact of high-k materials on the performance of DG MOSFETs, transistors. Figure of Merit in the sub threshold region (like threshold voltage, sub threshold slope and drain induced barrier Lowering); linear region (mobility and output resistance) and saturation region (normalized transconductance, early voltage) are analyzed for different high-k dielectric materials. The doping concentration of source and drain are taken as $1 \times 10^{20}$ cm$^{-3}$ and also the doping concentration of the channel is taken as $1 \times 10^{15}$ cm$^{-3}$ (Mohan Kumar et al 2010). The DG MOSFET shows improved transconductance, early voltage and higher drive current. So in this chapter the effect of introduction of wide range of proposed high-k materials as gate oxide dielectrics on the DG MOSFET is analysed for various device level parameters. Then the suitability of nano scale DG MOSFET for circuit applications is also analyzed with the help of an inverter circuit. The simulation results prove that use of high-k materials in DG MOSFETs reduces the Off current and gives better controllability.

4.2. DEVICE STRUCTURE AND PARAMETERS

The technology parameters and the supply voltages used for device simulations are according to International Technology Roadmap for
Semiconductors, (ITRS 2010) for 45 nm node devices. The proposed technology nodes with specifications matching the ITRS requirements are shown in Table 4.1.

Table 4.1 Proposed technology nodes with specifications matching the ITRS requirements

<table>
<thead>
<tr>
<th>Gate Length $L_g$ (nm)</th>
<th>65</th>
<th>45</th>
<th>32</th>
<th>22</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin Width $W_{fin}$ (nm)</td>
<td>22</td>
<td>15</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>Gate Oxide Thickness $T_{ox}$ (nm)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>Spacer Length $L_{sp}$ (nm)</td>
<td>35</td>
<td>22</td>
<td>16</td>
<td>11</td>
</tr>
<tr>
<td>Work Function (eV)</td>
<td>4.4</td>
<td>4.35</td>
<td>4.32</td>
<td>4.28</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Fin height $H_{fin}$ (nm)</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
</tr>
</tbody>
</table>

The 2D schematic cross-sectional view of a DG MOSFET is shown in Figure 4.1. The front and back gate oxide thickness is 1.2 nm and the channel thickness is 15 nm.

![Image of 2D DG MOSFET](image)

Figure 4.1 Cross-sectional views of the 2D DG MOSFET
In the DG MOSFET, the gate work function is fixed at 4.577 eV to obtain the threshold voltage of 0.357 V at a drain voltage of 0.1 V.

The design of devices and circuits for ultralow-power applications is a challenging task in the industry. Analog circuits based on the sub threshold operation of the devices gained interest because of quick switching operation (Mohan Kumar et al 2009).

Device simulator DESSIS of Integrated Systems Engineering Technology Computer Aided Design (ISE TCAD Manuals 2006) is used for realization and analysis of all the devices used in this simulation. An enhanced slicer is used to observe the doping profile, the electric field and the carrier velocity along the channel. Simulations are performed for a wide range of high-k dielectric materials in the devices and circuits.

Table 4.2 Device dimensions of the DG MOSFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Device Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length</td>
<td>45 nm</td>
</tr>
<tr>
<td>Channel thickness</td>
<td>15 nm</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>1.2 nm</td>
</tr>
<tr>
<td>Source/Drain Doping</td>
<td>$10^{20}$/cm$^3$</td>
</tr>
<tr>
<td>Channel doping</td>
<td>$10^{15}$/cm$^3$</td>
</tr>
</tbody>
</table>

The quantum potential is introduced to include quantization effects in a classical device simulation. In the density-gradient transport approximation, the quantum potential is a function of the carrier densities and their gradients. The silicon thickness of 15 nm is considered in this DG MOSFET. In thin silicon films
(<15 nm) the energy bands split into sub bands and the electrons are redistributed in these several sub bands. Thus scattering effects become dominant in such devices. So devices with 15 nm film thicknesses will have only coulomb scattering as the dominant factor for mobility degradation (Manoj et al 2007) and hence in the simulations the effects of coulomb scattering, high-field saturation and normal electric field are included to take into account mobility degradation.

4.3. HIGH- K DIELECTRICS

To fulfil the scaling scenario as projected in the previous chapter it is widely believed that high-k materials are needed to replace SiO$_2$ in the CMOS technology. From the beginning of MOS devices technology, SiO$_2$ has been used as gate oxide because of its stable SiO$_2$/Si interface as well as its electrical isolation property (Bouazra et al 2008). The continued shrinking of the CMOS device size for higher speed and lower power consumption drives the conventional SiO$_2$ gate oxide approaching its thickness scaling limit (Krishna Kumar Bhuwalka et al). The dielectric between the plates passes a small amount of Off current. This introduces an equivalent series resistance and also the dielectric has an electric field strength limit, resulting high breakdown voltage. Thicker gate layer might be used which can reduce the Off current flowing through the structure as well as improving the gate dielectric reliability.

Severe direct tunnelling and reliability problem at extremely small thickness will set a barrier for this SiO$_2$ as gate oxide material. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby reduce drive current and increase device performance. As the thickness scales below 2 nm, Off current due to tunnelling increases drastically, leading to high power consumption and reduced device reliability. Replacing silicon-di-oxide gate dielectric with a high-k material allows increased gate capacitance which leads to less leakage effects. Alternative dielectric materials with a higher dielectric constant and thus larger physical thickness than SiO$_2$ will be required to reduce the gate oxide Off current (Lee et al 2005) and
provide high On current. High-k dielectric materials have EOT of 1.0 nm with negligible gate oxide leakage, desirable transistor threshold voltages for MOSFETs and transistor channel mobility close to those of SiO₂ (Manoj et al 2007).

The implementation of high-k materials in the DG MOSFETs improves the scalability and performance. A high-k material needs to provide good electrical stability, and also the amount of charge trapped in the high-k materials need to remain at a low level even after extended operation of a transistor. It should also be scalable, that provide an acceptable level of leakage and acceptable levels of electron and hole mobility at a reduced thickness. High-k materials satisfying these conditions may be advantageously employed for high performance semiconductor devices since Off current increases, further reduction of thickness of gate oxide material in MOSFET. So an alternative method to increase gate capacitance is altering the relative dielectric constant of the material by replacing silicon dioxide with a high-k dielectric material. In such a scenario, a thicker gate layer might be used which can reduce the Off current flowing through the structure.

For both future silicon and emerging non-silicon nano electronic transistors, high-k material is required for enabling continued equivalent gate oxide thickness scaling, high performance, and for controlling gate oxide Off current. In addition, high-k gate dielectric is required for successful demonstration of high performance logic transistors on high-mobility non-silicon substrates with high $I_{On} / I_{Off}$ ratios. The capacitive coupling between gate and substrate has been increased over the years by decreasing the gate-dielectric thickness down to sub 2 nm (Jung Han Kang et al 2009). Different materials have different abilities to hold charge in the devices. High-k materials, such as hafnium dioxide (HfO₂), Zirconium dioxide (ZrO₂) and Titanium dioxide (TiO₂) inherently have a dielectric constant above 3.9. And the same oxide dielectric material and their silicate alloys must have good thermal stability, sound interface qualities and so on (Huang et al 2010; Manoj et al 2007).
The alternative high-k dielectric materials and its dielectric constant value, energy band gap and the conduction and valence band offset are summarised in Table 4.3. The band gap of SiO$_2$ is large, i.e., $\sim$9 eV, with sufficiently large conduction and valence band offsets compared to the reported band gap of 5.16 eV to 7.8 eV for alternative gate dielectric material. The band gap of TiO$_2$ is 3.5 eV, which does not lie in the above specified band gap range as shown in Table 4.3. Because of less band gap for TiO$_2$ it is not preferred as a gate dielectric in the DG MOSFET. Nano sized ZrO$_2$ is found as the emerging alternate material for SiO$_2$ and being a metal oxide it is expected to be invariant with higher thermal expansion ratio when subjected to operation in a FET configuration (Rajesh Kumar et al 2011; Manoj et al 2007). So in this thesis and all the discussions it is suggested that the best and the optimum high-k material is the nano sized ZrO$_2$. The result analysis is made with the help of suitable and the best nano sized ZrO$_2$ as gate oxide dielectric material and also other various high-k materials in DG MOSFET.

Table 4.3 Comparison of alternate dielectric materials with SiO$_2$

<table>
<thead>
<tr>
<th>Dielectric Material</th>
<th>Dielectric Constant (k)</th>
<th>Energy Band Gap Eg (eV)</th>
<th>Conduction Band Offset $\Delta E_C$ (eV)</th>
<th>Valence Band Offset $\Delta E$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>9</td>
<td>3.5</td>
<td>4.4</td>
</tr>
<tr>
<td>Si$_3$N$_1$</td>
<td>7.5</td>
<td>5.3</td>
<td>2.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>10</td>
<td>6</td>
<td>3</td>
<td>4.7</td>
</tr>
<tr>
<td>LaAlO$_3$</td>
<td>15</td>
<td>5.6</td>
<td>1.6</td>
<td>3.2</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>25</td>
<td>5.8</td>
<td>1.4</td>
<td>3.3</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>25</td>
<td>6</td>
<td>1.5</td>
<td>3.4</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>40</td>
<td>3.5</td>
<td>1.1</td>
<td>1.3</td>
</tr>
</tbody>
</table>
Here the gate dielectric Silicon dioxide of the DG MOSFET is replaced with the various alternate dielectric materials and simulations are carried out to evaluate the device performance.

The reduction of threshold voltage with decreasing channel length and increasing drain voltage is widely used as an indicator of the SCEs in evaluating CMOS cutting edge technologies. This adverse threshold voltage roll-off effect is the most daunting road block in future MOSFET design (Pavanello et al 2005).

4.4 FLOW DIAGRAM OF THE SIMULATION:

The step by step flow of the simulation for the different works discussed in this thesis is depicted in Figure 4.2. The first step is the study of Dual material double gate transistor (DG-MOSFET). A DG-MOSFET is comprised of a conducting channel which is surrounded by gate electrodes on either side which ensures that no part of the channel is far away from the gate electrode. The two types of DG-MOSFETs are symmetric DG-MOSFETs, having identical gate electrode materials for the front and back, and asymmetric DG-MOSFETs, having different from top and bottom.

Designing the DMDG MOSFET and SHDG MOSFET using the sentaurus software is the next step. DMDG is designed in order to enhance the immunity against short channel effects. And DG-MOSFET is designed because it provides excellent control of short channel effects. This is because its structure utilizes a very thin body to eliminate sub-surface leakage paths between the source and drain.

The next step is to study the different high-K materials. These materials are extensively utilized as the gate oxide dielectric layer in devices such as MOSFET, TFT and memory elements. SiO₂ is the conventional gate dielectric used in the devices. Current research is focusing on the replacement of this SiO₂ by different high-K materials.
Study of Different DG MOSFETS Devices

Design DG MOSFET, DMDG MOSFET and SHDG MOSFET using SENTAURUS Structure Editor

Study of Different High-K Materials

Selection of High-k Material

Synthesis of Nano size Zro$_2$ and analyzed the material properties

Applying all High-K material properties into DG MOSFET, DMDG MOSFET and SHDG MOSFET in SENTAURUS Structure Editor

Simulate Devices using SENTAURUS Structure

Analyze various Device level parameters for DG MOSFET, DMDG MOSFET and SHDG MOSFET using Inspect and Techplot Tool

Construct the inverter circuit using the above simulated devices in SENTAURUS Structure Editor

Calculate inverter gain for the DG MOSFET, DMDG MOSFET and SHDG MOSFET for VLSI applications and Analyzed

Figure 4.2 Flow Diagram of the simulation
According to semiconductor industry association and the thickness of SiO$_2$ should be smaller than 10 Å. The use of thin SiO$_2$ layer is precluded by several leakage problems. So different high-k gate dielectric materials are preferred because they can suppress the leakage current and also provide sufficient drive current. Here the nanosize ZrO$_2$ material is synthesised using wet chemical method and its electrical properties were analyzed. Due to its superior physical and electrical properties it is selected as an alternate for conventional gate oxide material. Then the different high-k material properties are used in the DG-MOSFET, DMDG MOSFET and SHDG MOSFET devices and their performance were analyzed.

In the next step, devices are simulated using sentaurus structure editor. Sentaurus workbench is the primary graphical front end that integrates sentaurus simulation programs into one environment. It is used in the semiconductor industry to design, organize and run simulations. The resulting data can be used with statistical and spread sheet software. The various device level parameters are analyzed with respect to different dielectric material like electron velocity, electrostatic potential, lateral electric field, drain current, transconductance, transconductance generation factor and intrinsic gain for DG-MOSFET, DMDG MOSFET and SHDG MOSFET using inspect and techplot tool.

The inverter circuit is constructed using the above simulated devices in the sentaurus structure editor. Unlike regular resistor- MOSFET inverter, CMOS does not contain any resistors, and hence it is e power efficient. In the last step, the inverter gain for DG-MOSFET, DMDG MOSFET and SHDG MOSFET are calculated for various VLSI applications.
4.5. SIMULATION RESULTS AND DISCUSSIONS

The device is constructed and simulated using the ITRS data. Then the different analog parameters and digital parameters such as early voltage, intrinsic gain, drain induced barrier lowering, output resistance, $I_{On}$, $I_{Off}$ and $I_{On}/I_{Off}$ are analyzed for DG MOSFET. The various parameters of DG MOSFET are examined for different gate oxide dielectric material.

$I_d$ Vs $V_{ds}$ curves for different values of dielectric constants are shown in the Figure 4.3. The drain current is increased while keeping the gate voltage constant for different high-k dielectric materials. Drain current in the saturation region is $1.5 \times 10^{-10}$ A for a device which uses ZrO$_2$ as gate oxide dielectrics.

![Graph showing drain current vs drain voltage for different high-k materials](image)

Figure 4.3 Comparison of variation of drain current in n-channel DG MOSFETs with different high-k material as a function of drain to source voltage

The drain current of device with SiO$_2$ is only $1 \times 10^{-10}$ A. The variation of electron velocity along the channel which is related to intrinsic cut off frequency is shown in Figure 4.4.
The use of high-k materials causes an increase in the velocity of electron near the drain end. As the gate voltage increases, higher electron density is obtained in the channel because the local electric field is increased along the position of the channel. The DG MOSFET with ZrO$_2$ as gate oxide dielectric electron velocity near the drain end in the channel is $4 \times 10^8 \text{ } \mu\text{m/s}$ which is higher compared to the velocity of DG MOSFET using SiO$_2$ whose value is $0.5 \times 10^8 \text{ } \mu\text{m/s}$.

The results clearly show that the electron mobility is increased with the use of different high-k dielectric materials in DG MOSFET. Molybdenum is taken as the gate material so that the gate work function can be fixed at 4.577 eV to obtain the threshold voltage of 0.3 V at a drain voltage of 0.1 V (Mohan Kumar et al 2010).

Figure 4.4 Electron velocity variation along the channel thickness in DG MOSFETs with different high-k materials
The electrostatic surface potential of the DG MOSFET for various high-k dielectric materials is shown in Figure 4.5. The electrostatic potential increases near the source end of the channel. It is observed that the electrostatic potential along the channel increases by replacing the high-k dielectric material as a gate oxide material in DG MOSFET. The electrostatic potentials near the drain also increased leading to reduction in Drain Induced Barrier Lowering.

![Graph showing electrostatic surface potential along the channel in n-channel DG MOSFET.](image)

Figure 4.5 Comparison of electrostatic surface potential along the channel in n-channel DG MOSFET.

The variation of the lateral electric field along the channel for different high-k dielectric material is shown in Figure 4.6.

It is evident from Figure 4.6 that the devices with high dielectric constant gate oxide material also have higher electric field along the channel for DG MOSFET. The electric field along the channel is increased for nano sized ZrO$_2$ in
comparison to conventional SiO$_2$ as a dielectric material in DG MOSFET because the recombination takes place very fast in the interface junctions.

Figure 4.6 Comparison of lateral electric field along the channel in MOSFETs with different high-k materials

The drain current and the transconductance variation with the gate to source voltage for drain voltage of 2 V are shown in Figure 4.7.
Figure 4.7 Comparison of variation of drain current and transconductance in MOSFETs with different high-k dielectric materials as a function of gate to source voltage

It is clearly visible that the DG MOSFET device with high-k dielectric material as gate oxide results in increased drain current with more independency with the drain to source voltage in the saturation region.

It is observed that the drain current increases as the gate dielectric constant value increases in DG MOSFET. This increase in drain current further increases the transconductance value. Hence for same EOT, high-k dielectric material is a suitable solution to increase the drain current of the device. This denotes the higher early voltage and output resistance of DG MOSFET.

Another parameter to be mentioned is $g_m/I_d$ ratio or the transconductance generation factor (TGF) which is viewed as the available gain per unit value of power dissipation. The $g_m/I_d$ curve is shown in the Figure 4.8. In a MOS transistor, $g_m/I_d$ in weak inversion is maximum and degrades severely with increasing drain current in the strong inversion regime.
4.5.1 Analysis of different Analog device parameters of the DG MOSFETs

Various analog parameters are analysed for a DG MOSFET with different high-k dielectric materials as gate oxide.

Intrinsic gain and Output resistance are plotted against different high-k dielectric materials for DG MOSFET is shown in Figure 4.9.
Figure 4.9 Comparison of Intrinsic Gain and Output resistance for DG MOSFETs with different high-k dielectric materials

It is clearly observed from the graph that the impact of high-k dielectrics on DG MOSFETs increases the Output resistance of the device for ZrO$_2$ as oxide material compared with SiO$_2$ dielectric material. So this can be used in cascade amplifiers. It is observed that the intrinsic gain is 10 for DG MOSFET with SiO$_2$ as gate oxide material and 190 for ZrO$_2$ as gate oxide material for the same device, so it is clearly proved that DG MOSFET with nano sized ZrO$_2$ as gate oxide material can be used in amplifier circuit in communication systems. The effective field at the drain end, results in high DIBL and hot-carrier effects, which are the major effects in the case of the short-channel devices in single gate devices. For logic applications, DIBL plays an important role as device dimensions are scaled rigorously (Mohan Kumar et al 2010).
The DIBL co-efficient is computed as

\[
\text{DIBL} = \frac{V_{t,\text{lin}} - V_{t,\text{sat}}}{V_{dd} - V_{t,\text{lin}}}
\]  

Where \(V_{t,\text{lin}}\) and \(V_{t,\text{sat}}\) are the threshold voltages measured at linear and saturation region for drain voltages of 0.1 V and 1.2 V, respectively. The supply voltage of 1.2 V is taken as per the conventions of ITRS for 45 nm gate length in regard of logic applications. The DIBL is calculated in the sub threshold region and the values against different dielectric constants are shown in Figure 4.10. DIBL is reduced for the devices with high-k dielectric material as gate oxide in DG MOSFET.

It degrades heavily for ZrO\(_2\) as compared to SiO\(_2\) as gate oxide material. So the high-k dielectric material in DG MOSFET reduces the Off current due to less DIBL. High-k dielectric materials reduce the DIBL which leads to reduction in short channel effect in DG MOSFET transistors.

Hence the ratio of \(I_{On}\) and \(I_{Off}\) for higher high-k dielectric materials is maximum in DG MOSFET. So the device shows higher \(I_{On}/I_{Off}\) ratio at sub threshold region of operation which leads to faster switching operation. The \(I_{On}/I_{Off}\) ratio current are plotted against different high-k values in Figure 4.10.
It is seen that the ratio increases exponentially by replacing high-k dielectric materials as a gate oxide in the DG MOSFET device performance. The \( \frac{I_{\text{on}}}{I_{\text{off}}} \) ratio is increased for nano sized ZrO2 over SiO2, so it is also suitable for low power applications in VLSI circuits because of the faster switching operations.

The Off current (leakage current) and the On current is plotted for different high-k dielectric materials as gate oxide in DG MOSFET is shown in Figure 4.11. Even though a transistor is logically turned off, there is a non-zero Off current through the channel at the microscopic level. This current is known as the sub threshold leakage because it occurs when the gate voltage is below its threshold voltage.
Figure 4.11 Comparison of Off current and On current for ratio and n-channel DG MOSFET with different high-k dielectric materials.

It is found that the Off current is low for higher high-k dielectric material while replacing in SiO₂ gate oxide material in DG MOSFET. A high threshold voltage in the standby mode gives low Off current (\(I_{\text{Off}}\)) leads to low power consumption. Here the Off current calculated from the TCAD inspect tool for the DG MOSFET is \(0.6 \times 10^{-9}\) A at \(v_g=0.15\) V and drain voltage \(v_d=0.6\) V. Off current is the current that causes the less power dissipation during the Off state in the device. The value of the gate to drain capacitance increases with the increase in the dielectric constant. The gate to drain capacitance is higher for the material ZrO₂ whose dielectric strength is 40. The total amount of capacitance is equal to sum of all the intrinsic gate capacitances that is \(C_{gg} = C_{gd} + C_{gs}\). The Table 4.4 shows different values of capacitance for different values of dielectric constant material for DG MOSFET devices. The value of gate capacitance increases as the value of dielectric constant of the dielectric material is increased. Due do this increase in capacitance decreases the Off current in the DG MOSFET device.
Table 4.4 Comparison of $C_{gd}$, $C_{gs}$ and $C_{gg}$ of DG MOSFET for different gate dielectric materials

<table>
<thead>
<tr>
<th>Dielectric constant($k$)</th>
<th>Drain Capacitance ($C_{gd}$) fF</th>
<th>Source Capacitance ($C_{gs}$) fF</th>
<th>Gate Capacitance ($C_{gg}$) fF</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.9</td>
<td>0.1</td>
<td>0.525</td>
<td>1</td>
</tr>
<tr>
<td>7.5</td>
<td>0.2</td>
<td>0.563</td>
<td>1.1</td>
</tr>
<tr>
<td>10</td>
<td>0.3</td>
<td>0.578</td>
<td>1.15</td>
</tr>
<tr>
<td>15</td>
<td>0.4</td>
<td>0.598</td>
<td>1.2</td>
</tr>
<tr>
<td>25</td>
<td>0.5</td>
<td>0.623</td>
<td>1.25</td>
</tr>
<tr>
<td>40</td>
<td>0.6</td>
<td>0.643</td>
<td>1.3</td>
</tr>
</tbody>
</table>

4.5.2. Circuit applications

The CMOS inverting amplifier circuit using DG MOSFET device is shown in Figure 4.12.

Figure 4.12 A high gain CMOS inverting amplifier
In a CMOS amplifier, with n-channel and p-channel devices as the driver and load respectively, the Output resistance $R_o$ which in turn is determined from the early voltage $V_A$ of the p-channel devices plays a significant role in determining the performance of the circuit. The input output transfer characteristics obtained for the inverting amplifier is shown in the Figure 4.13.

![Figure 4.13 Comparison of Voltage transfer characteristics of CMOS Inverter with DG MOSFET with different high-k dielectric materials](image)

The width of the p-channel device ($p_W$) is chosen to be three times the width of the n-channel device ($n_W$) to match the sub threshold current of both the devices.

The gain is computed by calculating the slope of the voltage transfer characteristics and is summarised in the Table 4.5. It is evidently proved that SiO$_2$ as a gate oxide dielectric has a low gain of 0.59 and ZrO$_2$ as the gate oxide dielectric material in DG MOSFET inverting amplifier has a higher gain of 0.69. So the inverter circuit with nano sized ZrO$_2$ gate dielectric improves the circuit performance over SiO$_2$ gate oxide dielectric in DG MOSFET.
Table 4.5 Comparison of voltage gain of CMOS inverter with different high-k materials

<table>
<thead>
<tr>
<th>Dielectric Material</th>
<th>Dielectric Constant (k)</th>
<th>Voltage Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>3.9</td>
<td>0.59</td>
</tr>
<tr>
<td>Si₃N₁</td>
<td>7.5</td>
<td>0.64</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>10</td>
<td>0.65</td>
</tr>
<tr>
<td>LaAlO₃</td>
<td>15</td>
<td>0.67</td>
</tr>
<tr>
<td>HfO₂/ZrO₂</td>
<td>25</td>
<td>0.69</td>
</tr>
<tr>
<td>TiO₂</td>
<td>40</td>
<td>0.93</td>
</tr>
</tbody>
</table>

4.6. CONCLUSION

In this chapter the different device parameters in the sub threshold region with various high-k dielectric materials for DG MOSFET devices and their optimization have been studied. It is noted that the mobility of the charge carriers are increased in the DG MOSFET for high-k dielectric materials. Improvements in the drain current, transconductance, Output resistance and voltage gain for ZrO₂ dielectrics are observed over conventional dielectrics in DG MOSFET.

The CMOS amplifiers implemented with these DG MOSFET with different high-k dielectric material subsequently have larger voltage gain than conventional MOSFET. The DIBL is decreased by 80% for ZrO₂ compared to the conventional SiO₂. The Off current decreases by 74% for ZrO₂ compared to SiO₂. The Off current is decreased for replacing high-k material in DG MOSFET. The gain of the inverter increases for the same devices with higher values of dielectric constant.
The gain of the amplifier increases by 16% for the inverting amplifier designed using ZrO$_2$ as dielectric material for DG MOSFET. In the subsequent chapters, the analysis of Nano scale Gate Engineering technique and Channel Engineering based on DG MOSFETs are discussed.