CHAPTER 1
INTRODUCTION

1.1. CMOS SCALING AND VLSI

Since the invention of the first electronic calculation machine, increasing the speed and improving the package density in miniaturization has been a constant challenge to the microelectronics industry. Electronic devices have brought, and will bring in the future, a far increasing number of new functions to the basic computing systems such as fast data computing, telecommunication, and several kinds of actuations which are collectively fabricated on the same physical object named as the solid state circuit, the integrated circuit or the “chip”. Electronic devices are so small, that billions of basic functions are accessible in a hand held system. Moreover, their unit cost has been divided by more than a factor of 100 million over the past 30 years. The collective fabrication of electronic devices coupled with the increase in their speed has given a tremendous success in the field of Micro and Nano electronics. Linear scaling of the device dimensions to a quasi-nano meter level allows the building up of a complex system, integrated on a chip which drastically reduces their volume and power consumption per function, whilst tremendously increasing their speed.

At present, in high-performance processor technology, the physical gate length of a transistor is entering into the sub-100 nm regime with a gate oxide thinner than 20 Å. In research laboratories, transistors are being fabricated which might be the prototypes of the last generation of CMOS devices based on the conventional structures and materials.

Since SiO₂ has approached its physical limit, alternative dielectrics have been introduced in the devices, such as Si₃N₄ (k~7.5), Al₂O₃ (k~10), LaAlO₃ (k~15), HfO₂/ZrO₂ (k~25), TiO₂ (k~40), and their silicates, which meet stringent requirements including thermal stability, large band gap, and compatibility to conventional CMOS process. Dielectric materials with moderate dielectric constant (k~15-30) were preferred due to less Drain Induced Barrier Lowering (DIBL). It
was reported that there is an universal relation between high-k value and breakdown properties. It was explained that the material structure plays an important role in breakdown. As the end of Semiconductor Industry Association (SIA) roadmap is being approached, the double gate (DG) devices are considered to be one of the most promising technologies for the future microelectronics industry due to its excellent immunity to short channel effects and higher drive on current. Conventional scaling based on the reduction of feature sizes obviously cannot continue forever. The aggressive scaling of the CMOS technology in the deep submicrometer regime gives rise to the short channel effects (SCEs). The various undesirable SCEs are threshold voltage roll-off, channel length modulation, drain induced barrier lowering (DIBL), punch through, velocity saturation, increased subthreshold leakage, transconductance degradation, increased parasitic capacitances etc. Analog performance parameters like the intrinsic gain, transconductance generating factor, the early voltage, the output resistance etc. are greatly affected by the SCEs. The undesirable mobility degradation and increased parasitic capacitances also drastically reduce the device transconductance, the voltage gain and the noise performance. Another major concern with scaling is the increased off-state leakage current which in turn increases the power dissipation.

1.2. ITRS

The International Technology Roadmap for Semiconductor (ITRS), which was established by a group of experts, serves several purposes within the semiconductors ground field. Its main objective is to specify the device design parameter values as predicted for future device technology. In addition to that, it highlights the challenges that device scaling might face in the coming generations. The (ITRS) main projection in the MOSFET and frontend process areas is high performance while keeping the low power logic. A major element of semiconductor device production is devoted to the digital logic ICs as well as to the memory ICs. Key considerations are the performance, the power, and the density requirements. The main focus is the high speed and the low power, which drives the technology
forward. The approaches for reaching these goals are at different levels. For high performance logic such as microprocessors, the main objective is maximum chip speed, with a trade off relative to the Off current. For low power logic approaches such as for mobile systems, the objective is to obtain long operating time by minimizing the chip power dissipation, particularly the static power dissipation, with a trade off of reducing the MOSFET speed. Moreover, the aim of the Roadmap is to identify key technical requirements and challenges critical to sustain the historical scaling of CMOS technology (i.e., according to Moore’s Law), and to encourage the research and development to meet the challenges.

1.3 MOTIVATION FOR THE THESIS

For the last few years, the integration issues of the analog functions in the standard digital CMOS have been the topics of research for several microelectronics researchers (Razavi 2001; Pavanello et al 2002; Kranti et al 2004). Quite a few researchers have suggested novel device technologies to improve the performance of the MOS devices for the System-on-Chip (SOC) applications. Within the conventional CMOS process flow, many of these approaches need the gate work function engineering, channel doping optimization and the source/drain engineering for improving the mixed signal performance. The concept of a Dual-Material Gate technology is similar to what was achieved by applying a different gate-bias in split-gate (Shur et al 1989; Mohan Kumar et al 2010) structure. The challenge to satisfactorily realize the split-gate FET is the inherent fringing capacitance between the two metal gates which increases as the separation between them is reduced. The new gate structure is introduced as dual material gate (DMG)-MOSFET (Lond et al 1999). Unlike asymmetric structures employing the doping engineering in which the channel field distribution is continuous, the gate-material engineering with its different work functions introduces a field discontinuity along the channel, resulting in simultaneous transport enhancement and suppress the Short Channel Effects (SCEs) (Xing Zhou et al 2000).
Next, the use of the halo doping in the channel has been widely reported for controlling the short channel effects in the sub 100 nm regimes. This doping scheme is well known to decrease the DIBL and \( I_{\text{off}} \). On the other hand, the halo doping is also briefly reported for its poor drain conductance under the long channel conditions. These devices show higher carrier mobility and better short channel performance compared to the uniformly doped channel devices. However, due to their higher substrate doping, Super Steep Retrograde (SSR) devices show reduced drive currents below 0.1 μm technology nodes. In particular, during the late nineties, the Single Pocket (SP), also known as the Single Halo (SH) or the Lateral Asymmetric Channel (LAC) has been reported for excellent short channel performance in the deep sub-micron technologies (Kranti et al 2004; Pavanello et al 2002). The process for these devices is similar to the conventional halo doped device, except for the absence of halo at the drain side. These devices are primarily reported to exhibit the improved drive currents in digital circuits. These devices are also briefly characterized to show improvement in analog performance and the hot carrier reliability in the deeply scaled technologies. Once the scaling of a conventional MOS transistor with a SiO\(_2\) gate insulator slows down due to physical limits, then new materials such as the high-k gate dielectrics is introduced. All recent studies indicate that the ultra-thin body double gate (DG) SOI MOSFET is the ideal device structure for the ultimate scaling in an ultra-thin body DG MOSFET; the second gate electrode can significantly suppress the SCEs.

1.4. SCOPE OF THE THESIS

The alternative device structure such as a double-gate MOSFET leads to improvement in the device performance. According to the device scaling physics, increasing the channel doping concentration (\( N_A \)) can effectively suppress the SCEs in the double-gate MOSFETs. The integration of high-k dielectric material in the devices has also shown a tremendous improvement in the DG-MOSFETs (FinFETs).
The work systematically investigates the device parameters for low power applications of n-channel advanced DG MOSFETs devices in 45 nm gate length. Channel Engineering technique (Lateral asymmetric channel) and Gate Engineering technique (Dual Material Gate) have been realized on the double gate MOSFET (FinFET) and investigated with different high-k materials.

For decades silicon dioxide is an excellent dielectric due to (i) the high quality interface between Si and SiO₂, (ii) chemical and thermal stability at high temperature (~1000 °C), (iii) good quality of insulation (iv) the property of hard mask in different diffusion and doping process and (v) high breakdown fields of 13 mV/cm. It is required to keep high capacitance density for channel formation in the sub-micron MOSFET with ultra-thin SiO₂ layer. The recent trend shows that the high Off current will prevent the scaling of the SiO₂ below 1 nm for future applications. Therefore, thickness reduction of SiO₂ gate layer below 1 nm is a big challenge. Again defects are formed in the gate oxide at the SiO₂/Si interface due to flow of charge carriers. If defect density reaches a certain threshold, this may cause quasi-breakdown on the gate layer. This is an important reliability issue of the transistor. An insulator with higher dielectric constant can be a solution.

But the alternative insulator should have the following properties : (i) chemical and electrical stability on silicon, (ii) uniform oxide thickness during fabrication, (iii) high breakdown voltage, (iv) thermal stability up to 1000 °C, (v) pinhole free and negligible defects, (vi) low charge trapping and ionic impurities, (vii) high life time under normal operating conditions, (viii) low interface state density for high carrier mobility, (ix) small gate-leakage current (x) low hot-carrier degradation, (xi) low diffusivity of boron and phosphorous at typical processing conditions. Here alternative dielectric material is suggested to replace the SiO₂ in different DG MOSFETs and it is found that the performance is superior for ZrO₂ over conventional dielectric material. The performance of the circuit is also discussed in the thesis.

Integrated Systems Engineering (ISE) - Technology Computer-Aided Design (TCAD) has been used for the realization and the analysis of all the devices
used in this study. All the device parameters are set as per ITRS road map for the 45 nm gate length. The Channel Engineered DG-MOSFETs and Gate Engineered DG-MOSFETs with different gate oxide high-k material are studied. And the nano sized ZrO$_2$ dielectric material which proves to be the best alternative for conventional SiO$_2$, is also shown in the DG MOSFET devices. Analog parameters like transconductance ($g_m$), transconductance generation factor ($g_m/I_d$), output resistance and the intrinsic gain of all the devices with different high-k materials have been investigated and compared with that of the conventional high-k material.

1.5. ORGANIZATION OF THE THESIS

The thesis is organized as stated below:

Chapter 2 deals with literature review of different high-k dielectric materials and the different device structures like DG MOSFET, DMDG MOSFET and SHDG MOSFET of the device proposed in this work.

Chapter 3 describes Synthesis of Nano sized high-k dielectric material for DG MOSFET using dry chemical process. The X-Ray Diffraction is taken for the Zirconia material and the particle size is also analyzed using scanning electron microscope. The impedance analysis method is followed to find the dielectric value of the material.

Chapter 4 discusses about the conventional DG MOSFET constructed using the ITRS roadmap and the device dimensions. Then the different high-k dielectric material is replaced in the device instead of conventional gate oxide material. The various device parameters are analyzed with respect to different dielectric material like electron velocity, electrostatic potential, lateral electric field, drain current, transconductance, transconductance generation factor, intrinsic gain, output
resistance, DIBL, On current, Off current and $I_{\text{on}}/I_{\text{off}}$ ratio. The gain is also calculated for the DG MOSFET based inverter for circuit applications.

Chapter 5 investigates about the Gate Engineered Double Gate MOSFET. The DMDG MOSFET device is constructed based on the specification from ITRS roadmap. Then the SiO$_2$ is replaced by different high-k material in the DMSG MOSFET device. The various device parameters are analyzed for DMDG MOSFET with respect to different high-k dielectric material; the parameters are electron velocity, electrostatic potential, lateral electric field, drain current, transconductance, transconductance generation factor, intrinsic gain, output resistance, DIBL, On current, Off current and $I_{\text{on}}/I_{\text{off}}$ ratio. The gain is also calculated for the DMDG MOSFET with different high-k material based inverter for the circuit applications.

Chapter 6 deals with the Channel Engineered Double Gate MOSFET constructed using the ITRS roadmap and the device dimensions. The Channel Engineered DG MOSFETs conventional gate oxide material is replaced by different high-k material and the analysis is made here. The various device parameters like electron velocity, electrostatic potential, lateral electric field, drain current, transconductance, transconductance generation factor, intrinsic gain, output resistance, DIBL, On current, Off current and $I_{\text{on}}/I_{\text{off}}$ ratio are also discussed in this chapter. The gain is also calculated for the inverter for the circuit applications.

Chapter 7 gives the conclusions of the present work and summaries future enhancements.